

Garda-D Block Diagram

IDT CV125PA
 (ICS 954206) 3

Yonah 478

1.83G/2G/2.16G_{4.5}

19

-1M-0111

PCB P/N : 55.4A901.XXX

REVISION : 05217-1

(Hannstar, ACCL)

PCB STACKUP

2

S

VCC

1

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INPUTS	OUTPUTS
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DCBATOUT	5V_s5 3D3V_s5
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SYSTEM DC/DC
TPS51124 41

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100		43
1D8X S3	DDR VREF S0	

APL5332KAC	43
3D3H G0	3D5H G0

APL5912-U		43
125M 12	125M 12	

MAXIM CHARGER
MAX8725 42

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
ISL6262 28 20

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 143

ATI M54 DC/DC
FAN5234 52

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

APL5331KAC		43
120W 50	120W 50	

<Variant Name>

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Size

A3

Date: Wednesday, January 11, 2006

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ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
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ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+ -0.25 Center
1	0	0	1	+ -0.5 Center
1	0	1	0	+ -0.75 Center
1	0	1	1	+ -1.0 Center
1	1	0	0	+ -0.25 Center
1	1	0	1	+ -0.5 Center
1	1	1	0	+ -0.75 Center
1	1	1	1	+ -1.0 Center

page 3

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->G, B->B, C->F, D->G,	0
MiniPCI	21	A/C B/D -> E	1
LAN	23	A -> H	2

History

Calistoga Strapping Signals and Configuration

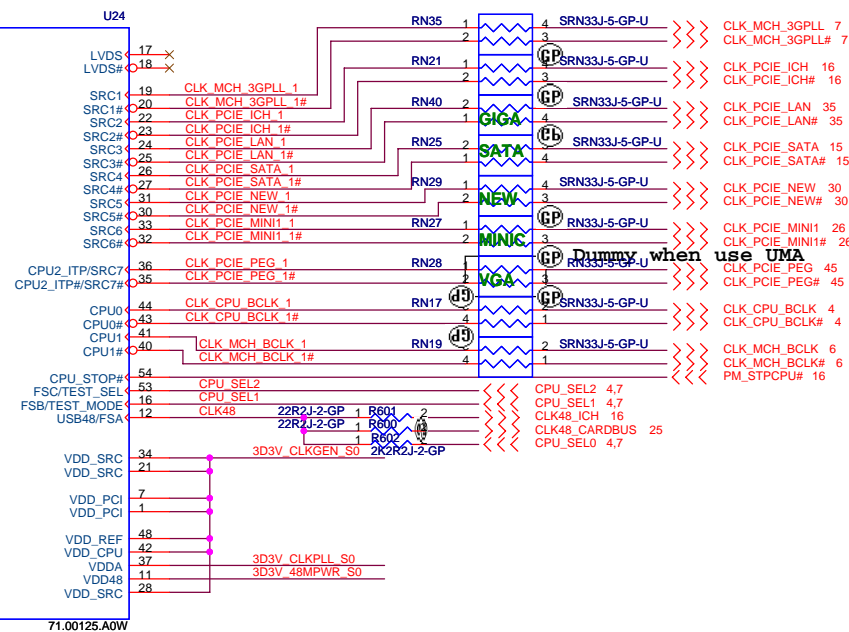
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

<Variant Name>

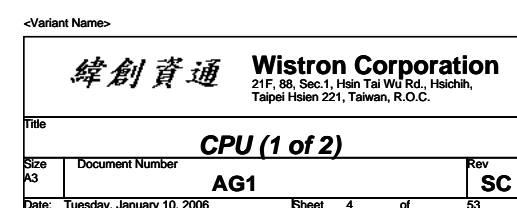
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Title			
Reference			
Size	Document Number	Rev	
A3	AG1	SD	
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SEL2	SEL1	SEL0	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X



VCC_CORE_S0

VCC_CORE_S0

U72C

A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD9
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AE19
D10	VCC[027]	VCC[094]	AE10
D12	VCC[028]	VCC[095]	AE12
D14	VCC[029]	VCC[096]	AE14
D15	VCC[030]	VCC[097]	AE15
D17	VCC[031]	VCC[098]	AE17
D18	VCC[032]	VCC[099]	AE18
E7	VCC[033]	VCC[100]	AE20
E9	VCC[034]	VCC[034]	
E10	VCC[035]	VCCP[01]	V6
E12	VCC[036]	VCCP[02]	G21
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	K21
F7	VCC[041]	VCCP[07]	M21
F9	VCC[042]	VCCP[08]	N21
F10	VCC[043]	VCCP[09]	N6
F12	VCC[044]	VCCP[10]	R21
F14	VCC[045]	VCCP[11]	R6
F15	VCC[046]	VCCP[12]	T21
F17	VCC[047]	VCCP[13]	T6
F18	VCC[048]	VCCP[14]	V21
F20	VCC[049]	VCCP[15]	W21
AA7	VCC[050]	VCCP[16]	
AA9	VCC[051]	VCCA	B26
AA10	VCC[052]	VCCA	
AA12	VCC[053]	VCCA	
AA13	VCC[054]	VCCA	
AA15	VCC[055]	VCCA	
AA17	VCC[056]	VCCA	
AA18	VCC[057]	VCCA	
AA20	VCC[058]	VCCA	
AB9	VCC[059]	VCCA	
AC10	VCC[060]	VCCA	
AB10	VCC[061]	VCCA	
AB12	VCC[062]	VCCA	
AB14	VCC[063]	VCCA	
AB15	VCC[064]	VCCA	
AB17	VCC[065]	VCCA	
AB18	VCC[066]	VCCA	
	VCC[067]	VCCA	

AB20	VCC[068]	VCC[068]	AB20
AB7	VCC[069]	VCC[069]	AB7
AC7	VCC[070]	VCC[070]	AC7
AC9	VCC[071]	VCC[071]	AC9
AC12	VCC[072]	VCC[072]	AC12
AC13	VCC[073]	VCC[073]	AC13
AC15	VCC[074]	VCC[074]	AC15
AC17	VCC[075]	VCC[075]	AC17
AC18	VCC[076]	VCC[076]	AC18
AD7	VCC[077]	VCC[077]	AD7
AD9	VCC[078]	VCC[078]	AD9
AD10	VCC[079]	VCC[079]	AD10
AD12	VCC[080]	VCC[080]	AD12
AD14	VCC[081]	VCC[081]	AD14
AD15	VCC[082]	VCC[082]	AD15
AD17	VCC[083]	VCC[083]	AD17
AD18	VCC[084]	VCC[084]	AD18
AE9	VCC[085]	VCC[085]	AE9
AE10	VCC[086]	VCC[086]	AE10
AE12	VCC[087]	VCC[087]	AE12
AE13	VCC[088]	VCC[088]	AE13
AE15	VCC[089]	VCC[089]	AE15
AE17	VCC[090]	VCC[090]	AE17
AE18	VCC[091]	VCC[091]	AE18
AE20	VCC[092]	VCC[092]	AE20
AE19	VCC[093]	VCC[093]	AE19
AE10	VCC[094]	VCC[094]	AE10
AE12	VCC[095]	VCC[095]	AE12
AE14	VCC[096]	VCC[096]	AE14
AE15	VCC[097]	VCC[097]	AE15
AE17	VCC[098]	VCC[098]	AE17
AE18	VCC[099]	VCC[099]	AE18
AE20	VCC[100]	VCC[100]	AE20

1D05V_S0

Layout Note

R285
0R0402-PAD

C369

SCD1U10V2KX-4GP

1D05V_VCCA_S0

1D05V_S0

L22

HCB1608KF121T30-GP

68.00230.041

C673

SC4D7U6D3V3KX-GP

C674

SCD01U10V2KX-3GP

VCC_CORE_S0

R300

100R2F-L1-GP-U

VCC_SENSE 38

VSS_SENSE 38

R298

100R2F-L1-GP-U

VCC_CORE_S0

Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:

Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

VCC_CORE_S0

C715

SC10U10V5ZY-1GP

C346

SC10U10V5ZY-1GP

C344

SC10U10V5ZY-1GP

C343

SC10U10V5ZY-1GP

C701

SC10U10V5ZY-1GP

C713

SC10U10V5ZY-1GP

C702

SC10U10V5ZY-1GP

C714

SC10U10V5ZY-1GP

C703

SC10U10V5ZY-1GP

C877

SC10U10V5ZY-1GP

C370

SC10U10V5ZY-1GP

C683

SC10U10V5ZY-1GP

C712

SC10U10V5ZY-1GP

C366

SC10U10V5ZY-1GP

C678

SC10U10V5ZY-1GP

U72D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
A26	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U21
B19	VSS[014]	VSS[095]	U24
B21	VSS[015]	VSS[096]	V2
B24	VSS[016]	VSS[097]	V5
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C22	VSS[023]	VSS[104]	Y6
C25	VSS[024]	VSS[105]	Y21
D1	VSS[025]	VSS[106]	Y24
D11	VSS[026]	VSS[107]	AA2
D13	VSS[027]	VSS[108]	AA5
D16	VSS[028]	VSS[109]	AA8
D18	VSS[029]	VSS[110]	AA11
D19	VSS[030]	VSS[111]	AA14
D23	VSS[031]	VSS[112]	AA16
D26	VSS[032]	VSS[113]	AA19
E3	VSS[033]	VSS[114]	AA22
E6	VSS[034]	VSS[115]	AA25
E8	VSS[035]	VSS[116]	AB1
E11	VSS[036]	VSS[117]	AB4
E14	VSS[037]	VSS[118]	AB8
E16	VSS[038]	VSS[119]	AB11
E19	VSS[039]	VSS[120]	AB13
E21	VSS[040]	VSS[121]	AB16
E24	VSS[041]	VSS[122]	AB19
F5	VSS[042]	VSS[123]	AB23
F8	VSS[043]	VSS[124]	AB26
F11	VSS[044]	VSS[125]	AC3
F13	VSS[045]	VSS[126]	AC6
F16	VSS[046]	VSS[127]	AC8
F19	VSS[047]	VSS[128]	AC11
F22	VSS[048]	VSS[129]	AC14
F25	VSS[049]	VSS[130]	AC16
G4	VSS[050]	VSS[131]	AC19
G1	VSS[051]	VSS[132]	AC21
G23	VSS[052]	VSS[133]	AC24
G26	VSS[053]	VSS[134]	AD2
H3	VSS[054]	VSS[135]	AD8
H6	VSS[055]	VSS[136]	AD11
H21	VSS[056]	VSS[137]	AD13
H24	VSS[057]	VSS[138]	AD16
J2	VSS[058]	VSS[139]	AD19
J5	VSS[059]	VSS[140]	AD22
J22	VSS[060]	VSS[141]	AE1
J25	VSS[061]	VSS[142]	AE4
K1	VSS[062]	VSS[143]	AE8
K4	VSS[063]	VSS[144]	AE11
K23	VSS[064]	VSS[145]	AE14
K26	VSS[065]	VSS[146]	AE16
L3	VSS[066]	VSS[147]	AE19
L6	VSS[067]	VSS[148]	AE23
L21	VSS[068]	VSS[149]	AE26
L24	VSS[069]	VSS[150]	AF3
M2	VSS[070]	VSS[151]	AF6
M5	VSS[071]	VSS[152]	AF9
M22	VSS[072]	VSS[153]	AF11
M25	VSS[073]	VSS[154]	AF13
N1	VSS[074]	VSS[155]	AF16
N4	VSS[075]	VSS[156]	AF19
N23	VSS[076]	VSS[157]	AF21
N26	VSS[077]	VSS[158]	AF24
P3	VSS[078]	VSS[159]	
	VSS[079]	VSS[160]	
	VSS[080]	VSS[161]	
	VSS[081]	VSS[162]	

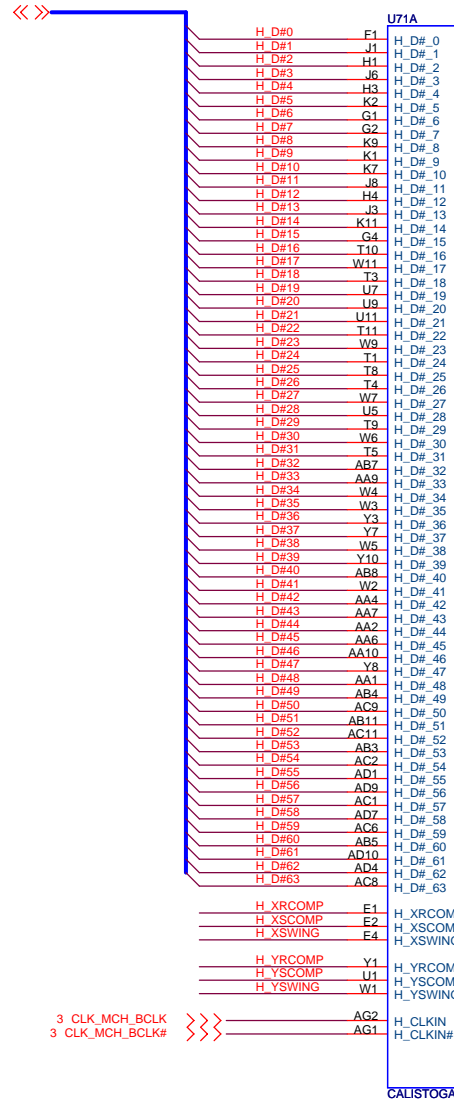
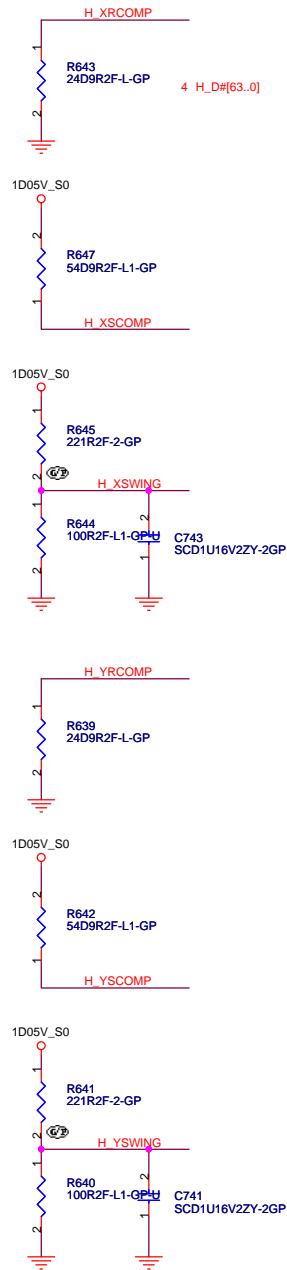
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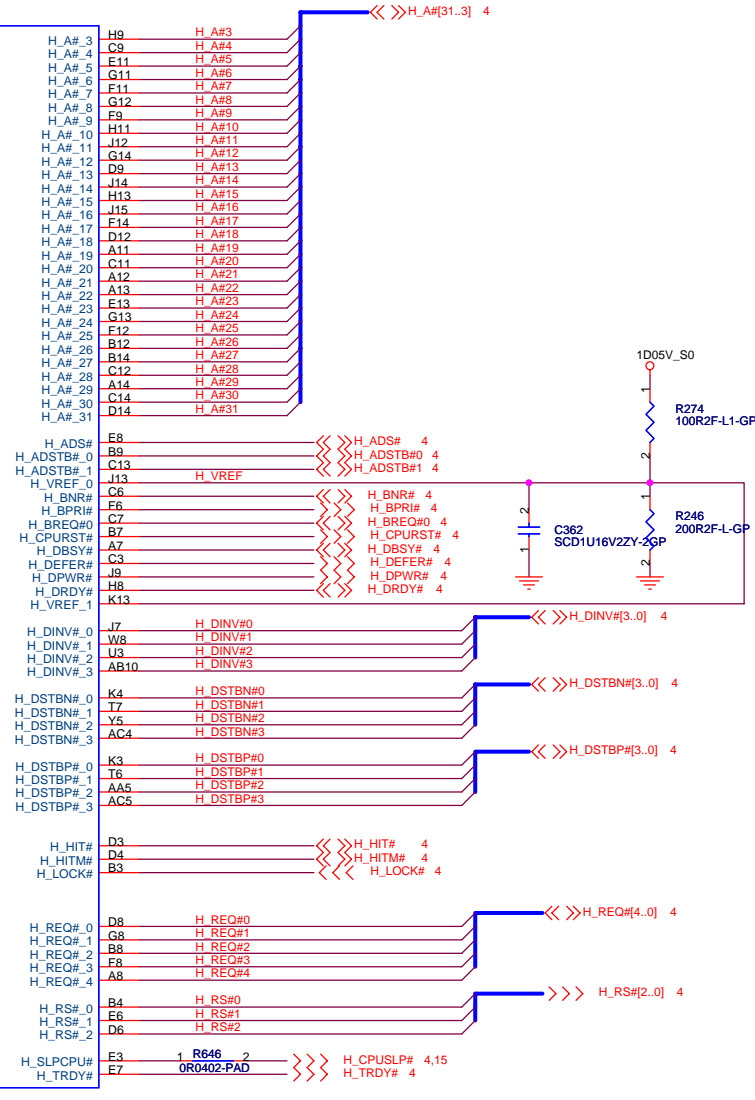
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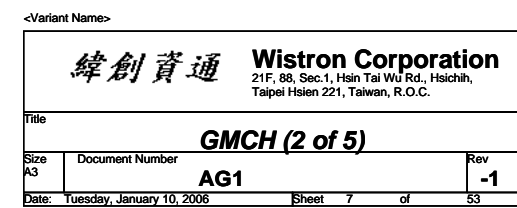


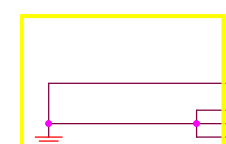
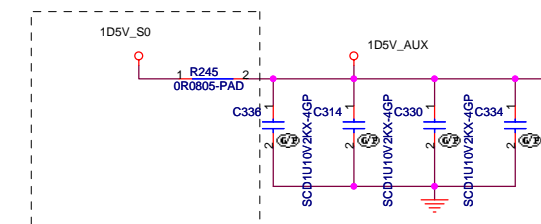
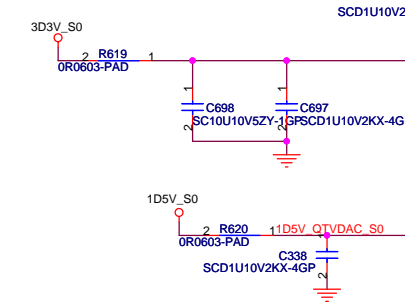
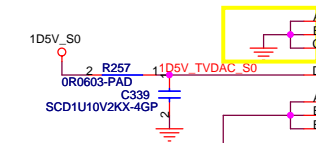
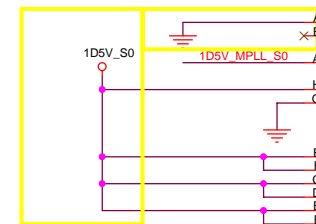
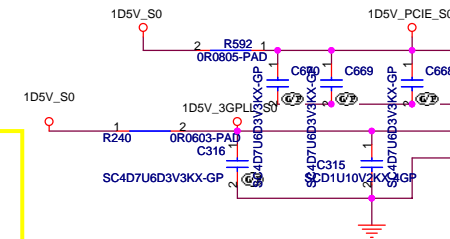
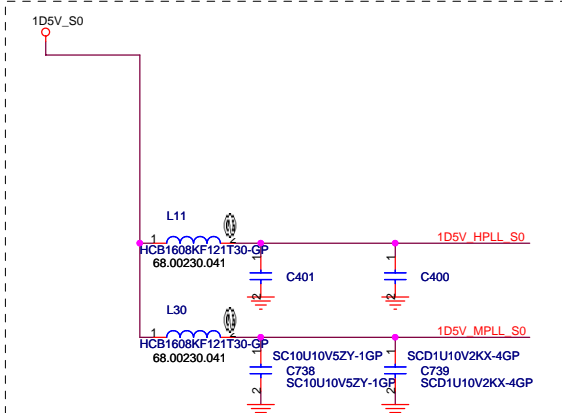
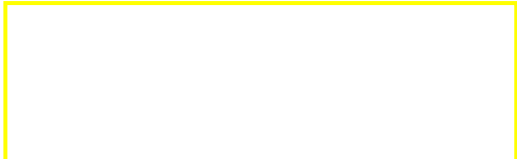
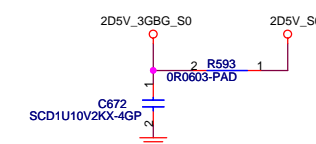
Place them near to the chip (< 0.5")

<Variant Name>

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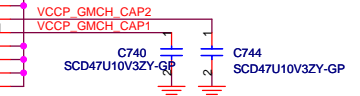
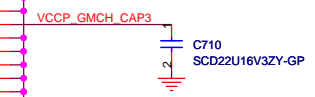
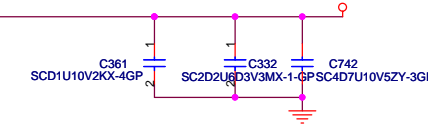




- U71H**
- VCCSYNC
 - VCC_TXLVDS0
 - VCC_TXLVDS1
 - VCC_TXLVDS2
 - VCC3G0
 - VCC3G1
 - VCC3G2
 - VCC3G3
 - VCC3G4
 - VCC3G5
 - VCC3G6
 - VCCA_3GPLL
 - VCCA_3GBG
 - VSSA_3GBG
 - VCCA_CRTDAC0
 - VCCA_CRTDAC1
 - VSSA_CRTDAC
 - VCCA_DPLLA
 - VCCA_DPLLB
 - VCCA_HPLL
 - VCCA_LVDS
 - VSSA_LVDS
 - VCCA_MPLL
 - VCCA_TVBG
 - VSSA_TVBG
 - VCCA_TVDACA0
 - VCCA_TVDACA1
 - VCCA_TVDACB0
 - VCCA_TVDACB1
 - VCCA_TVDACC0
 - VCCA_TVDACC1
 - VCCD_HMPLL0
 - VCCD_HMPLL1
 - VCCD_LVDS0
 - VCCD_LVDS1
 - VCCD_LVDS2
 - VCCD_TVDC
 - VCC_HV0
 - VCC_HV1
 - VCC_HV2
 - VCCD_QTVDC
 - VCCAUX0
 - VCCAUX1
 - VCCAUX2
 - VCCAUX3
 - VCCAUX4
 - VCCAUX5
 - VCCAUX6
 - VCCAUX7
 - VCCAUX8
 - VCCAUX9
 - VCCAUX10
 - VCCAUX11
 - VCCAUX12
 - VCCAUX13
 - VCCAUX14
 - VCCAUX15
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 - VCCAUX17
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 - VCCAUX30
 - VCCAUX31
 - VCCAUX32
 - VCCAUX33
 - VCCAUX34
 - VCCAUX35
 - VCCAUX36
 - VCCAUX37
 - VCCAUX38
 - VCCAUX39
 - VCCAUX40

POWER

- VTT_0
- VTT_1
- VTT_2
- VTT_3
- VTT_4
- VTT_5
- VTT_6
- VTT_7
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- VTT_76

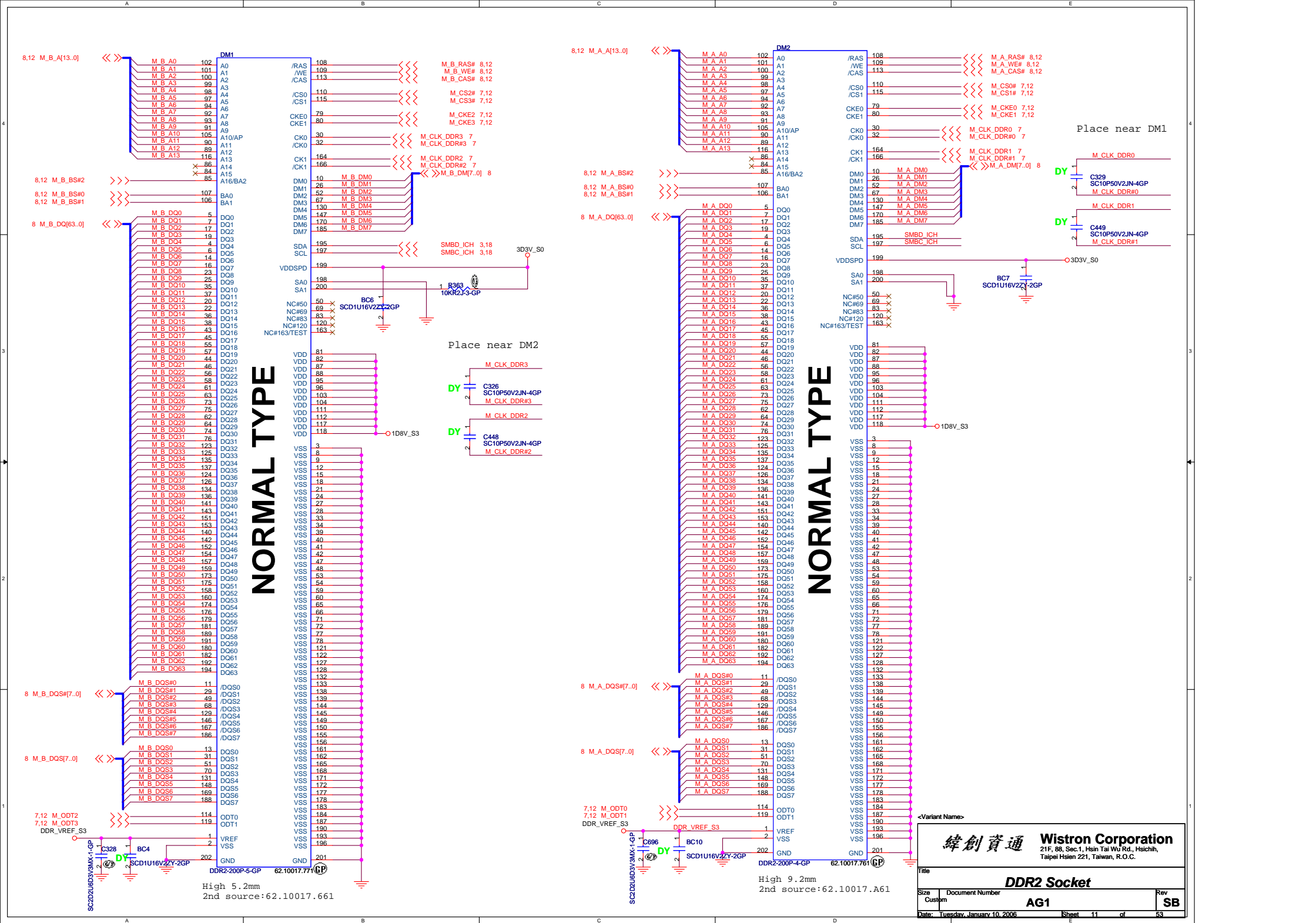


<Variant Name>

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Title: **GMCH (4 of 5)**

Size A3	Document Number AG1	Rev SA
Date: Tuesday, January 10, 2006		Sheet 9 of 53



DDR_VREF_S0

Put decap near power(0.9V) and pull-up resistor

Diagram illustrating the connection of a DDR memory array to a VREF line. The array consists of 16 rows of memory cells (RN55 to RN67) connected to a common VREF line. Each row has four data lines (1-4) and four address lines (A0-A3). The diagram shows the internal structure of the memory cells and the connections to the VREF line. The VREF line is connected to the common source of the memory cells. The address lines are connected to the word lines of the memory cells. The data lines are connected to the bit lines of the memory cells. The diagram also shows the pull-up resistors and decoupling capacitors connected to the VREF line.

Key components and connections shown:

- Memory cells: RN55, RN62, RN60, RN59, RN54, RN61, RN63, RN65, RN66, RN56, RN64, RN67.
- Address lines: M_A_A12, M_B_A9, M_A_A9, M_B_A8, M_B_A5, M_B_A3, M_B_A1, M_B_A10, M_B_A13, M_B_A0, M_B_A2, M_B_A4, M_B_A6, M_B_A7, M_B_A11, M_A_A0, M_A_A2, M_A_A4, M_A_A6, M_A_A7, M_A_A11, M_A_A5, M_A_A3, M_A_A1, M_A_A10.
- Data lines: M_CKE2 7,11, M_B_BS#2 8,11, M_ODT1 7,11, M_ODT3 7,11, M_ODT2 7,11, M_CS2# 7,11, M_B_RAS# 8,11, M_B_BS#1 8,11, M_CKE3 7,11, M_B_BS#0 8,11, M_B_WE# 8,11, M_CS3# 7,11, M_B_CAS# 8,11, M_ODT0 7,11, M_CS0# 7,11, M_A_RAS# 8,11, M_A_BS#1 8,11, M_A_BS#0 8,11, M_A_WE# 8,11, M_A_CAS# 8,11, M_CS1# 7,11, M_CKE0 7,11, M_A_BS#2 8,11, M_CKE1 7,11, M_A_A5, M_A_A3, M_A_A1, M_A_A10.
- Control signals: M_CKE2 7,11, M_B_BS#2 8,11, M_ODT1 7,11, M_ODT3 7,11, M_ODT2 7,11, M_CS2# 7,11, M_B_RAS# 8,11, M_B_BS#1 8,11, M_CKE3 7,11, M_B_BS#0 8,11, M_B_WE# 8,11, M_CS3# 7,11, M_B_CAS# 8,11, M_ODT0 7,11, M_CS0# 7,11, M_A_RAS# 8,11, M_A_BS#1 8,11, M_A_BS#0 8,11, M_A_WE# 8,11, M_A_CAS# 8,11, M_CS1# 7,11, M_CKE0 7,11, M_A_BS#2 8,11, M_CKE1 7,11.

*Put decap near power(0.9V)
and pull-up resistor*

The diagram shows a PCB layout for the DDR3 VREF_S0 signal. It features two horizontal signal traces, one for the top and one for the bottom. Each trace is populated with a series of decoupling capacitors (C435, C419, C413, C387, C386, C411, C384, C412, C438, C385, C391 on the top; and C418, C396, C415, C434, C436, C398, C397, C409, C408, C407, C437 on the bottom). The capacitors are labeled with their values (e.g., 22µF, 10µF, 100nF) and footprints (e.g., SCD1U16V22, SCD1U16V10, SCD1U16V100). Pull-up resistors (R435, R419, R413, R387, R386, R411, R384, R412, R438, R385, R391 on the top; and R418, R396, R415, R434, R436, R398, R397, R409, R408, R407, R437 on the bottom) are placed near the capacitors. The layout is connected to a power plane (VDD_0.9V) and a ground plane (GND). The text "Put decap near power(0.9V) and pull-up resistor" is written above the layout.

Place these Caps near DM1

1D8V_S3

C734 SC2D2U6D3V3MX-1-GP

C735 SC2D2U6D3V3MX-1-GP

C394 SC2D2U6D3V3MX-1-GP

C395 SC2D2U6D3V3MX-1-GP

C417 SC2D2U6D3V3MX-1-GP

C389 SCD1U16V2ZYSOP

C414 SCD1U16V2ZYSOP

C388 SCD1U16V2ZYSOP

C410 SCD1U16V2ZYSOP

16V2ZYSOP

Place these Caps near DM2

108V_S3

C733 SC2D2U6D3V3MX-1-GP

C392 SC2D2U6D3V3MX-1-GP

C390 SC2D2U6D3V3MX-1-GP

C759 SC2D2U6D3V3MX-1-GP

C761 SC2D2U6D3V3MX-1-GP

C382 SCD1U16V22V2Z2-2GP

C383 SCD1U16V22V2Z2-2GP

C416 SCD1U16V22V2Z2-2GP

C393 SCD1U16V22V2Z2-2GP

DM2

LAUNCH BD CONN

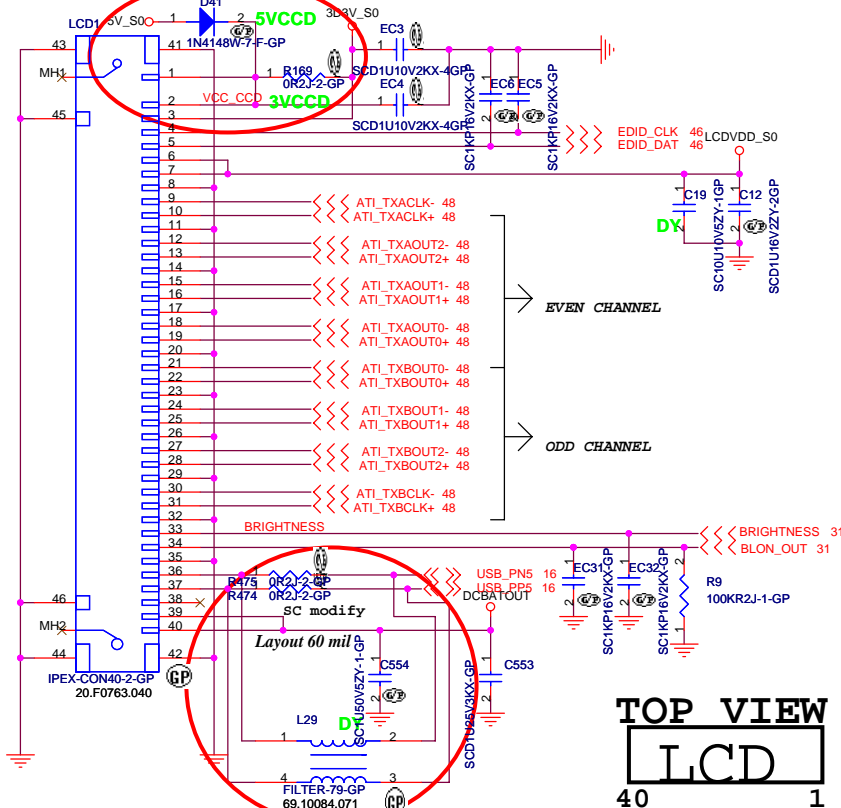


Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

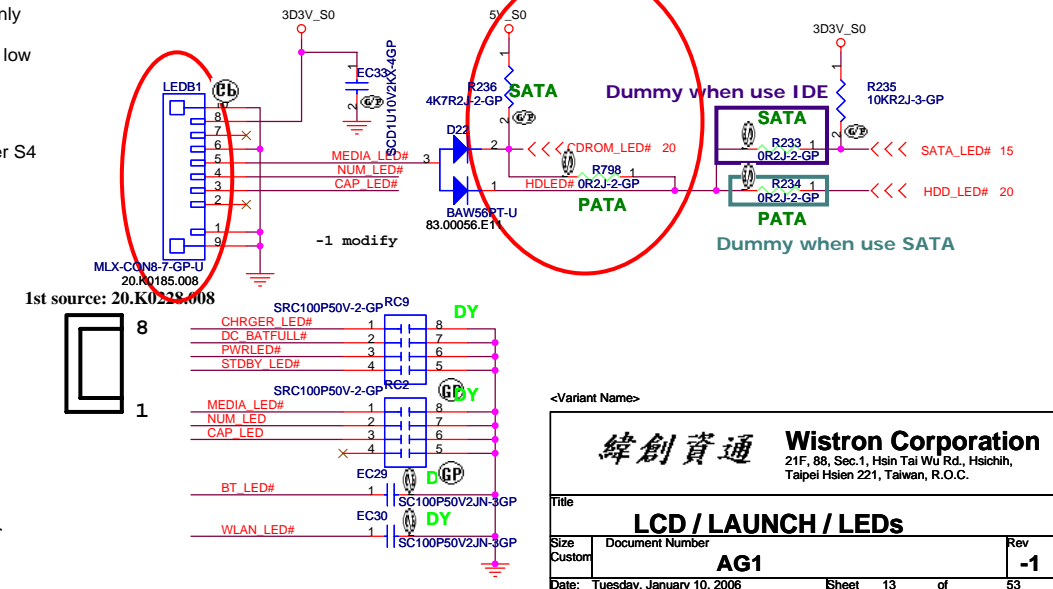
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICN

LCD/INVERTER/CCD CONN

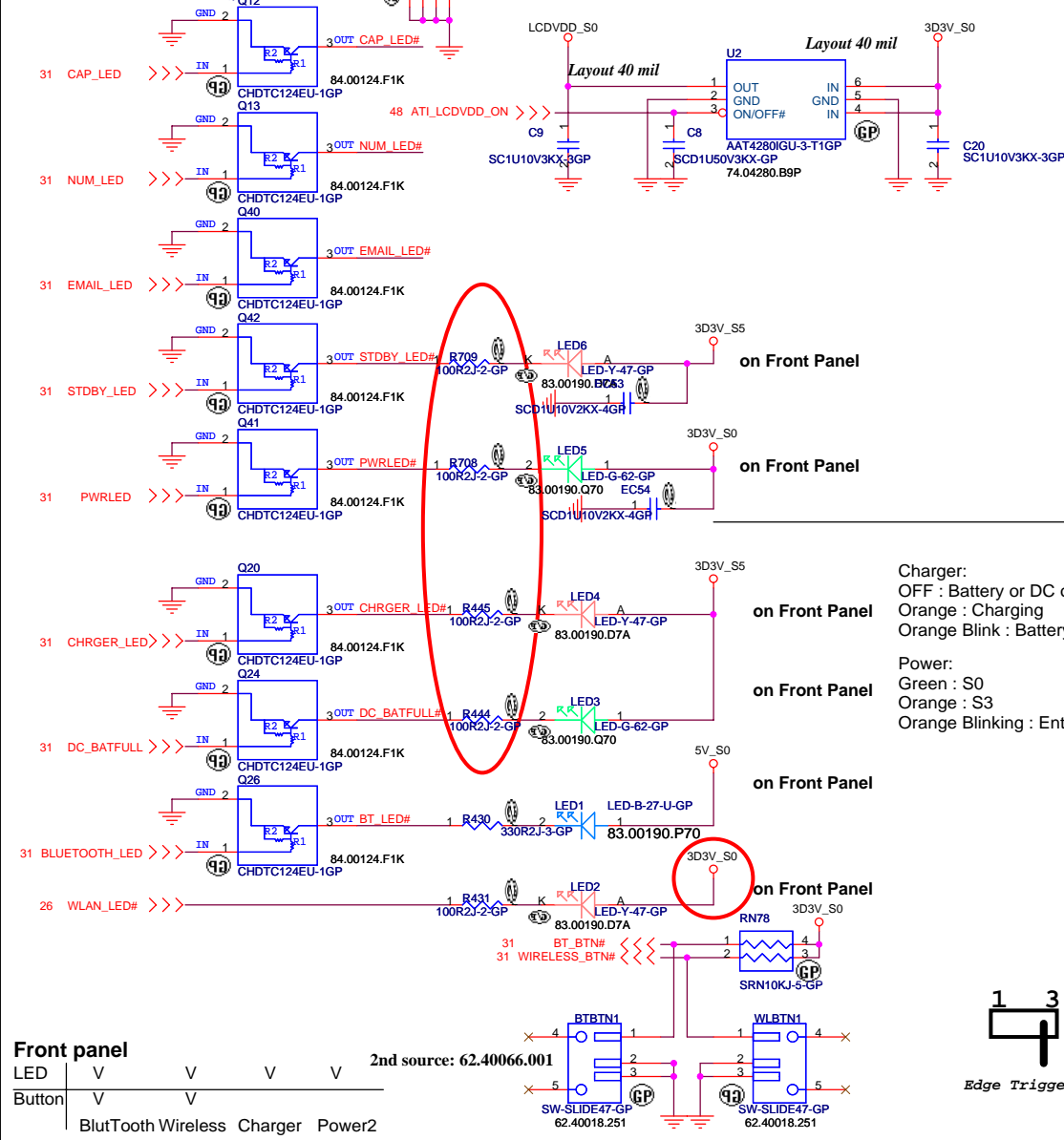


LED BD CONN

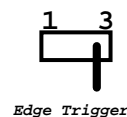


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LCD / LAUNCH / LEDs	
Title Size Custom	Document Number AG1
Date: Tuesday, January 10, 2006	Sheet 13 of 53

2nd source: 20.K0185.012



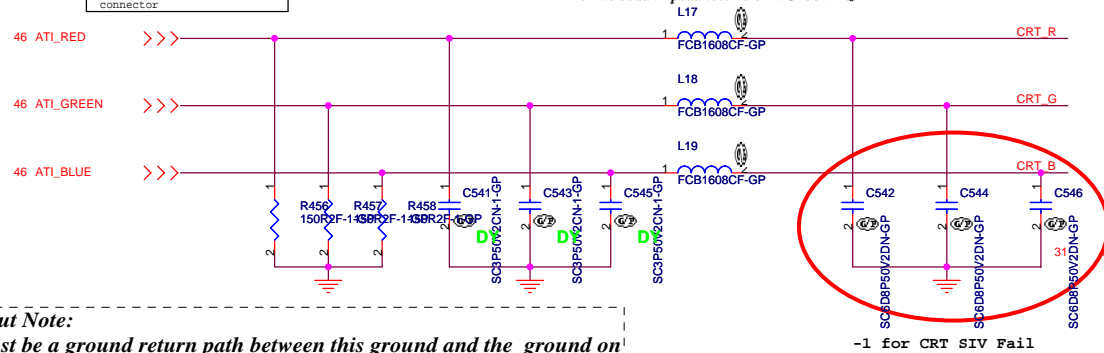
LED	V	V	V	V
Button	V	V	V	V
Bluetooth Wireless Charger Power2				



CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

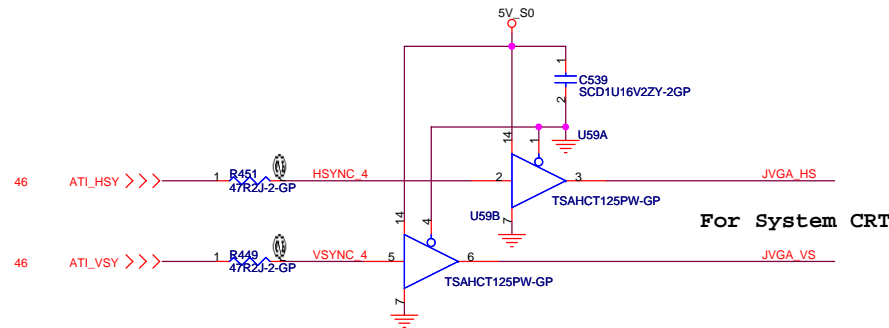
Ferrite bead impedance: 10 ohm@100MHz



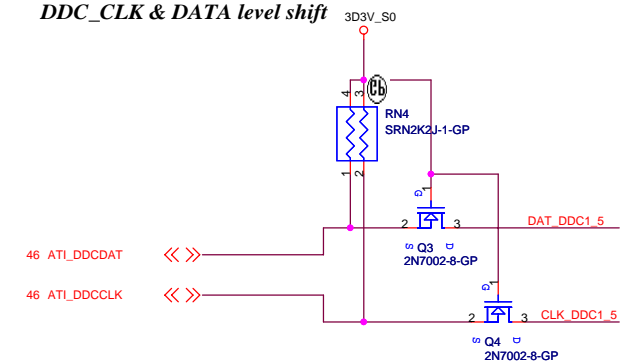
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



DDC_CLK & DATA level shift



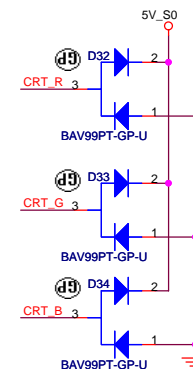
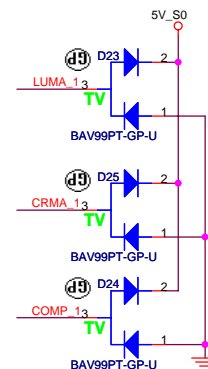
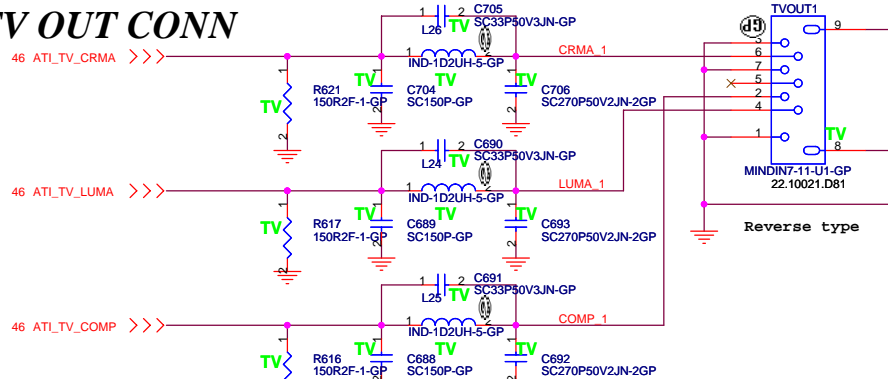
-1 for CRT SIV Fail

-1 for CRT SIV Fail

For System CRT

-1 for CRT SIV Fail

TV OUT CONN



<Variant Name>

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT/TV Connector

Size

Document Number

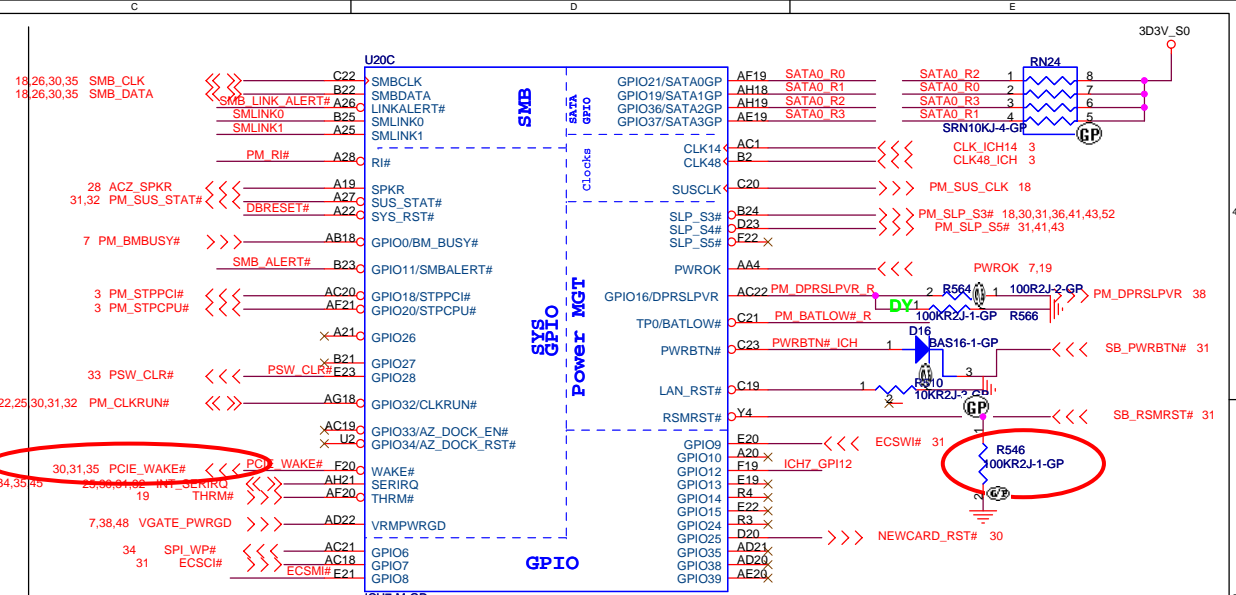
AG1

Rev

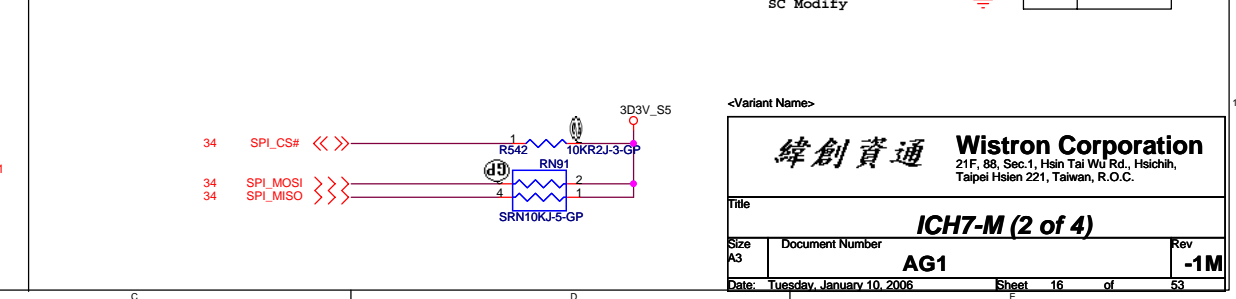
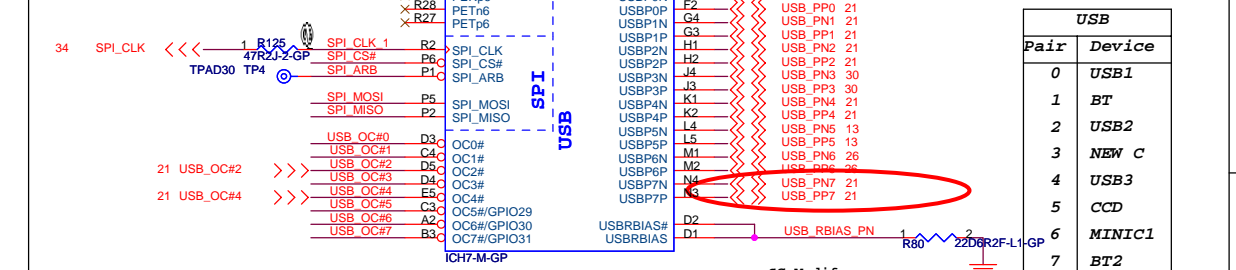
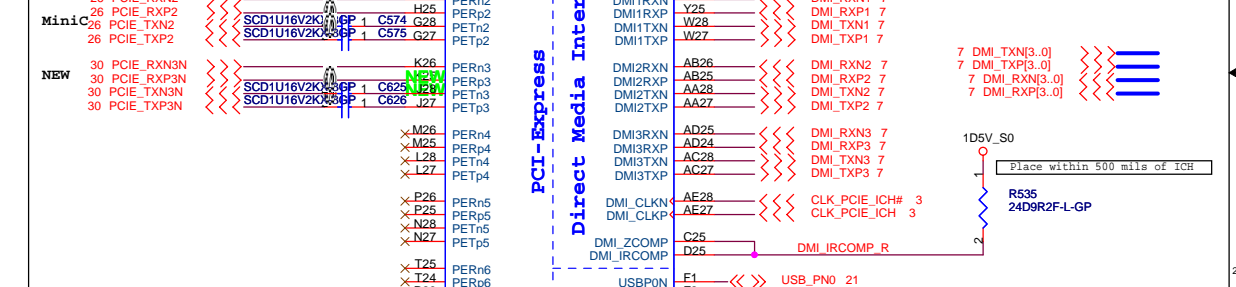
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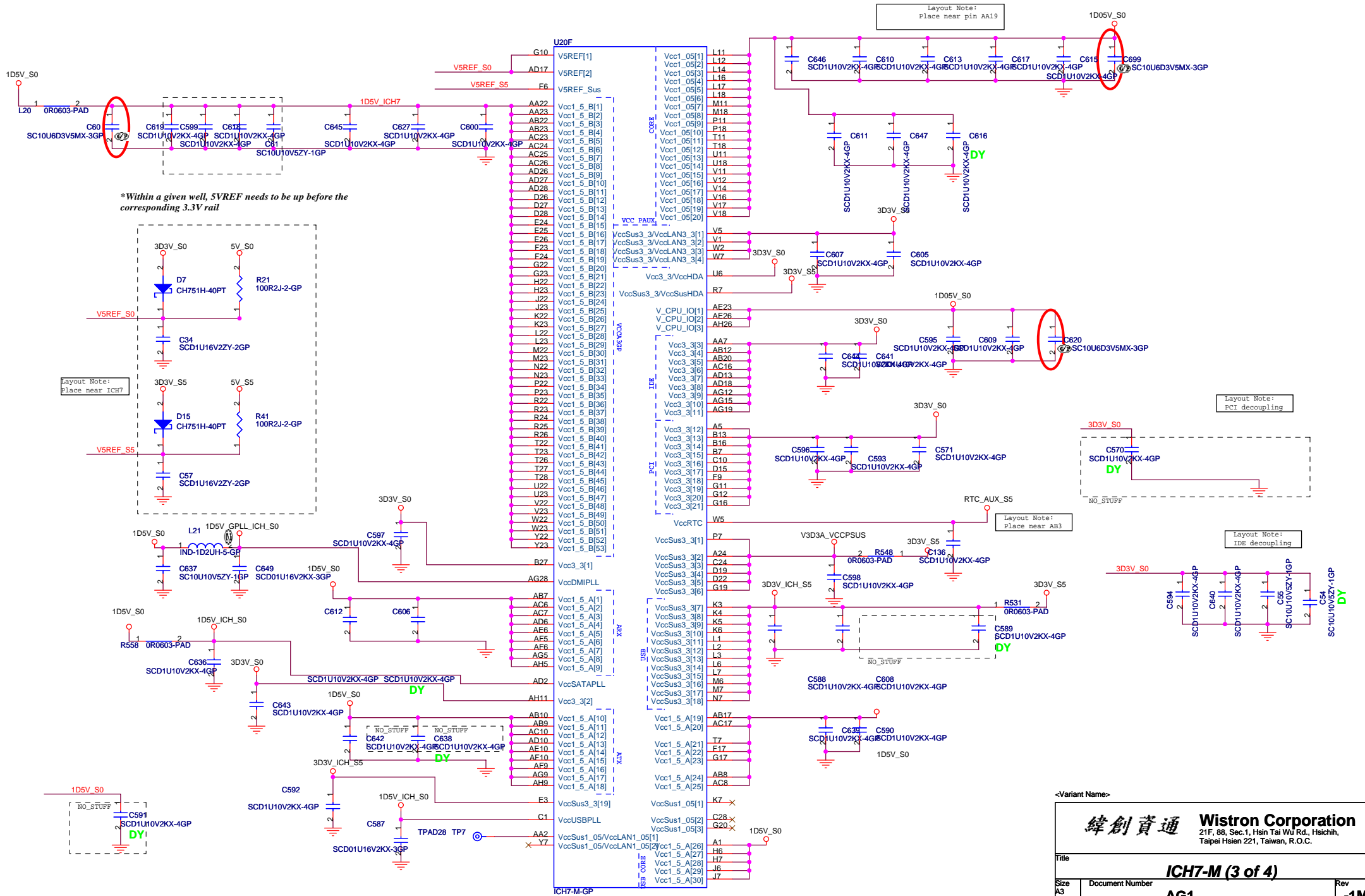
Date: Tuesday, January 10, 2006

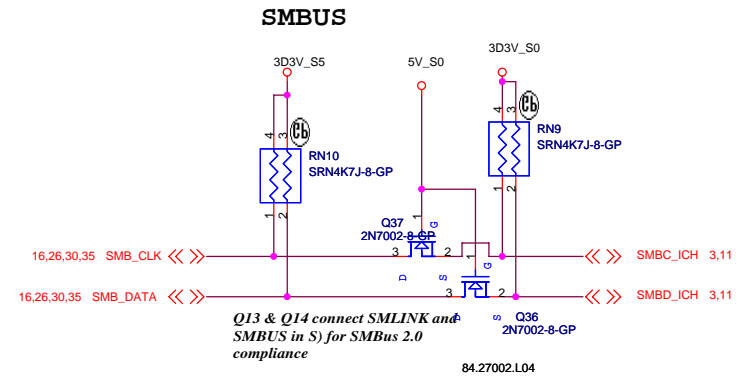
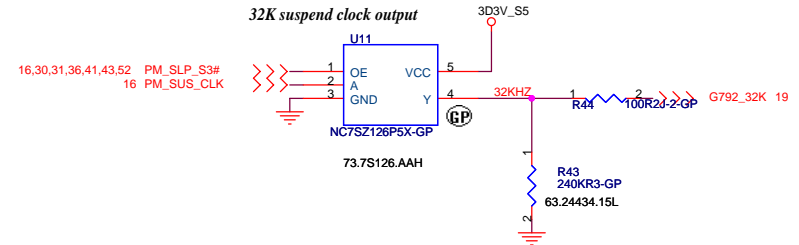
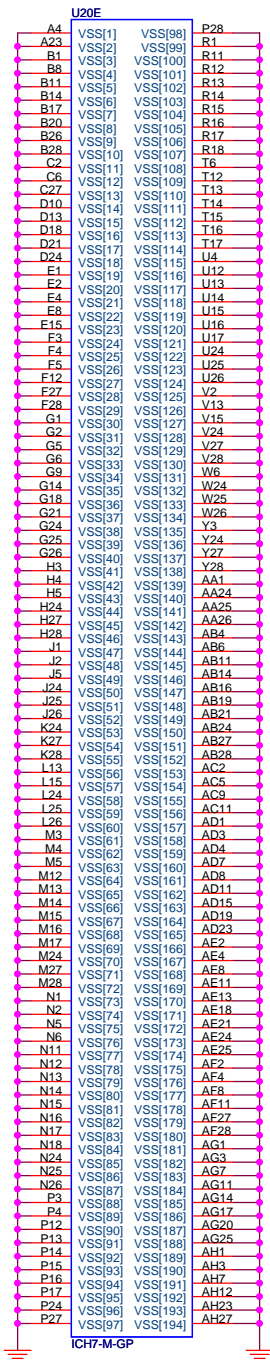
Sheet 14 of 53

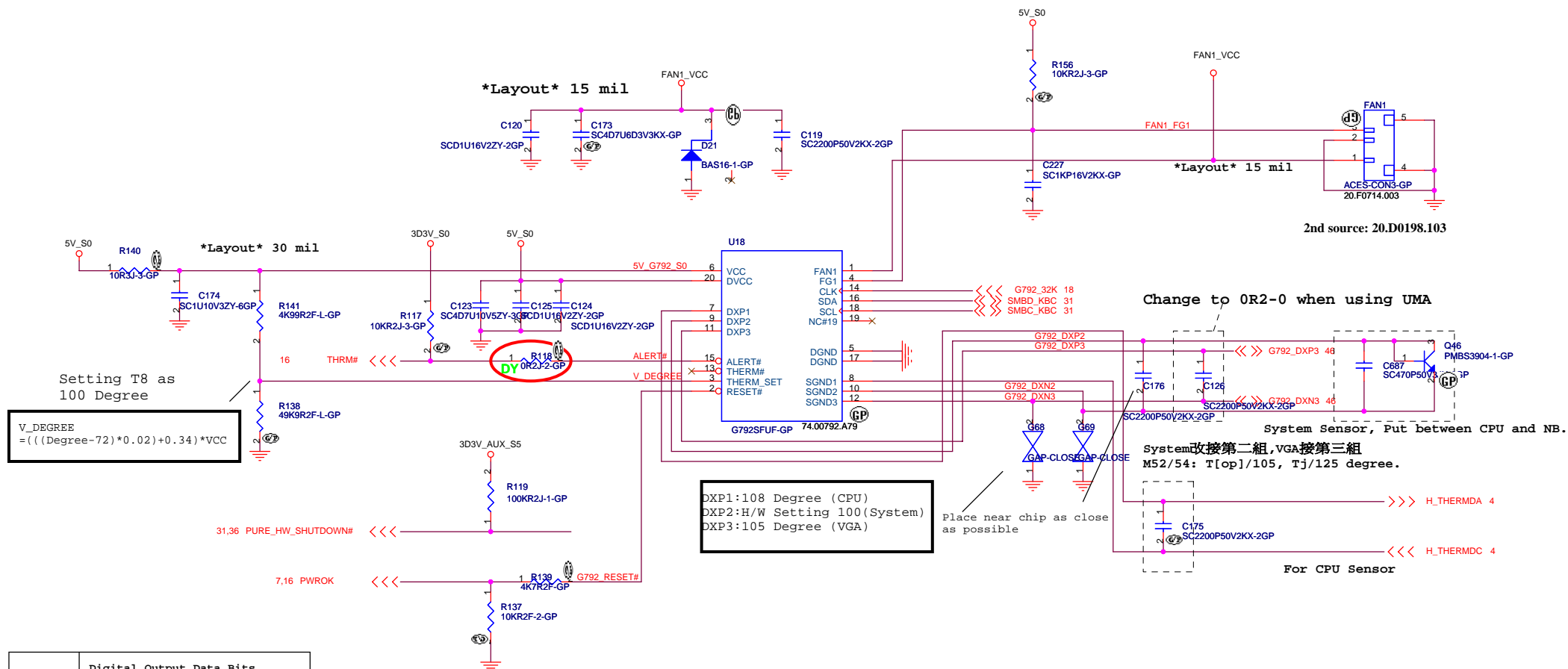


MiniC	26	PCIE_RXP2	SCD1U16V2K0	GP 1	C574	G28	PERn2	DM1RXN	Y25	DM1_RXP1	7
	26	PCIE_TXN2	SCD1U16V2K0	GP 4	C575	G27	PERp2	DM1RXP	W28	DM1_TXN1	7
	26	PCIE_TXN2	SCD1U16V2K0	GP 4	C575	G27	PETn2	DM1TXN	W27	DM1_TXN1	7

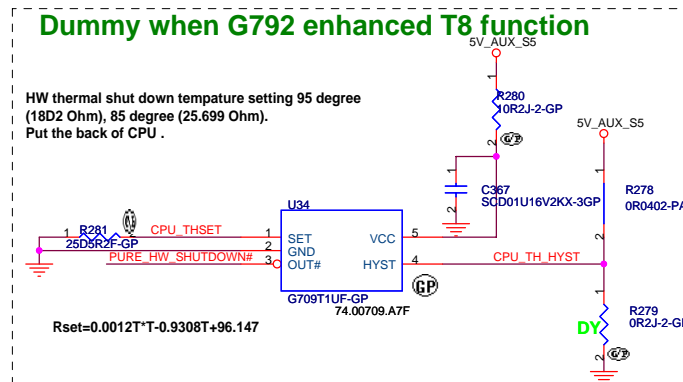








TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



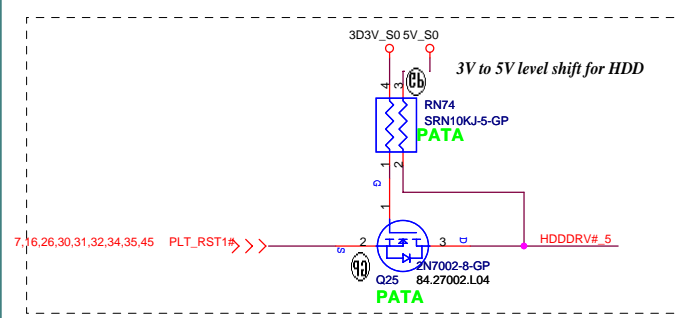
Thermal Get Setting

		T6	T7
Sensor 0	CPU DTS	98	100
Sensor 1	G792-1 CPU	98	100
Sensor 2	G792-2 System	78	83
Sensor 3	G792-3 VGA	110	115

<Variant Name>

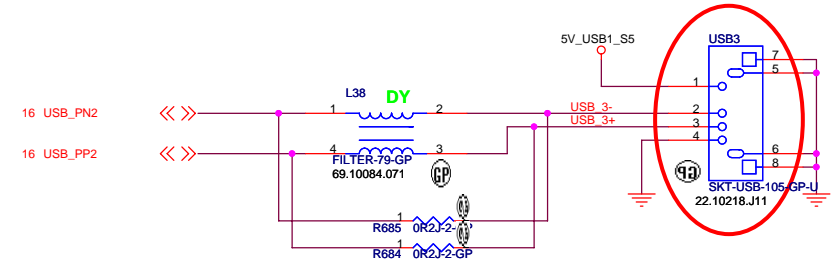
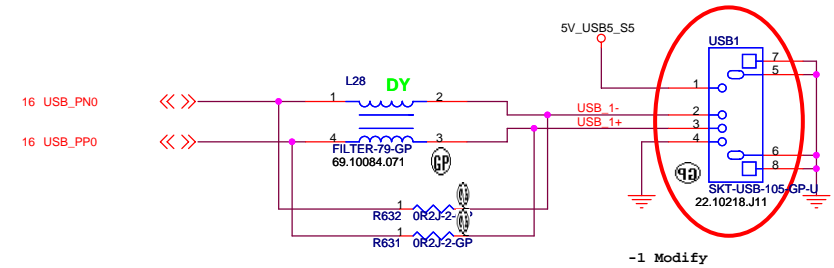
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Thermal/Fan Controller G792	
Title	Size	Document Number	Rev
	Custom	AG1	SC
Date: Tuesday, January 10, 2006	Sheet	19	of 53

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The diagram shows the CDROM1 connector with the following connections:

- IDE Signals:**
 - IDE_PDD8, IDE_PDD9, IDE_PDD10, IDE_PDD11, IDE_PDD12, IDE_PDD13, IDE_PDD14, IDE_PDD15, IDE_PDDREQ, IDE_PDIOREQ#
 - IDE_PDDACK#, IDE_PDA2, IDE_PDCS3#
 - IDE_PDD7, IDE_PDD6, IDE_PDD5, IDE_PDD4, IDE_PDD3, IDE_PDD2, IDE_PDD1
 - IDE_PDIOHW#, IDE_PDA1, IDE_PDA0, IDE_PDCS1#, CDROM_LED#
- SATA Signals:**
 - SATA_R374 (R2J2-2GP)
- CDROM Signals:**
 - CDROM1 (d3)
 - SPD-COMN50-4R-19GPU 20.80346.050
- Power and Ground:**
 - 3D3V_S0
 - 5V_S0
 - Ground
- Other Components:**
 - Capacitors: C131, C130
 - Resistor: RN23 SRN8K2J-3-GP
 - Inductor: Lb



15,28 ACZ_SDATOUT >>>
 15,28 ACZ_SYNC >>>
 15 ACZ_SDATIN1 >>>
 15,28 ACZ_RST# >>>

ACZ_DIN1 A R

AMP-CONN12A-GF

20.F0582.012

2nd source: 20.F0604.012

3D3V_LAN_S5

C564 SC1U10V3KX-3GP

R494 39R2J-1-GP

C562 SC22P50V2JN-4GP

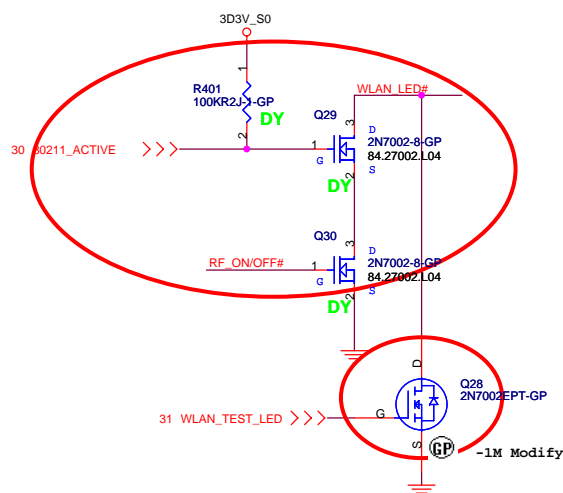
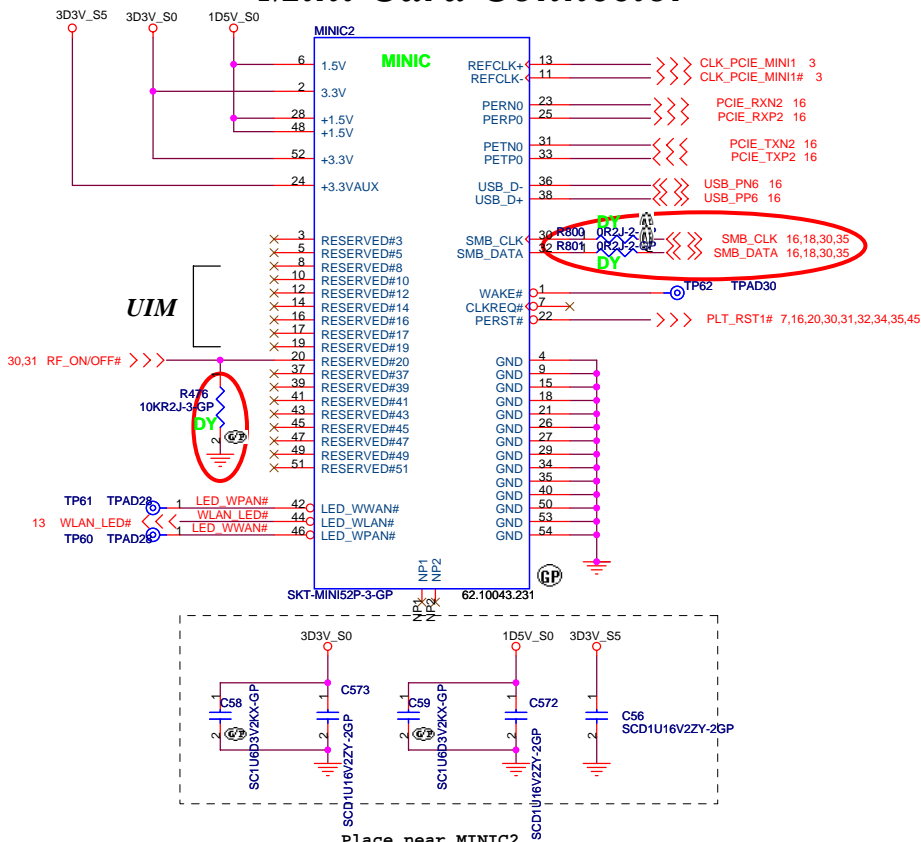
R495 100KR2J-1-GP

EC563 SC22P50V2JN-4GP

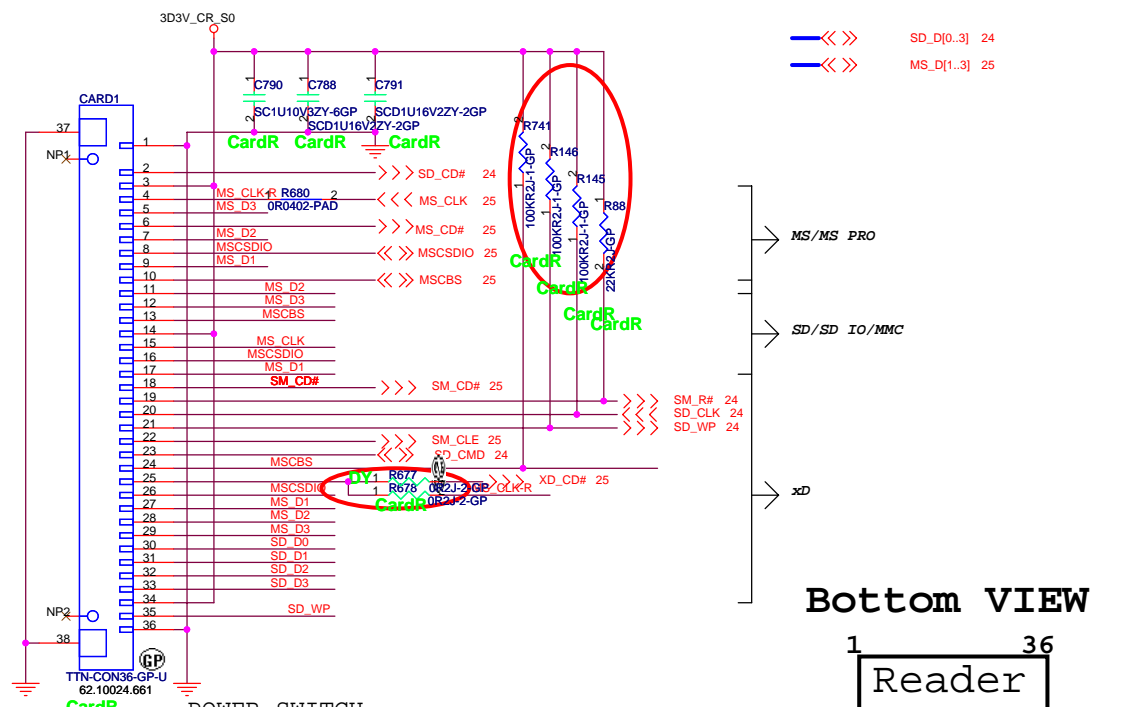
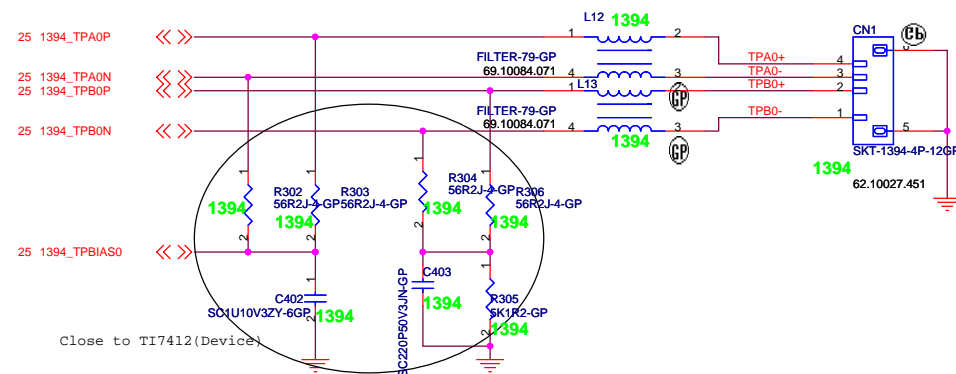
ACZ_BTCLK_MDC 15



Mini Card Connector



1394 Connector



Bottom VIEW

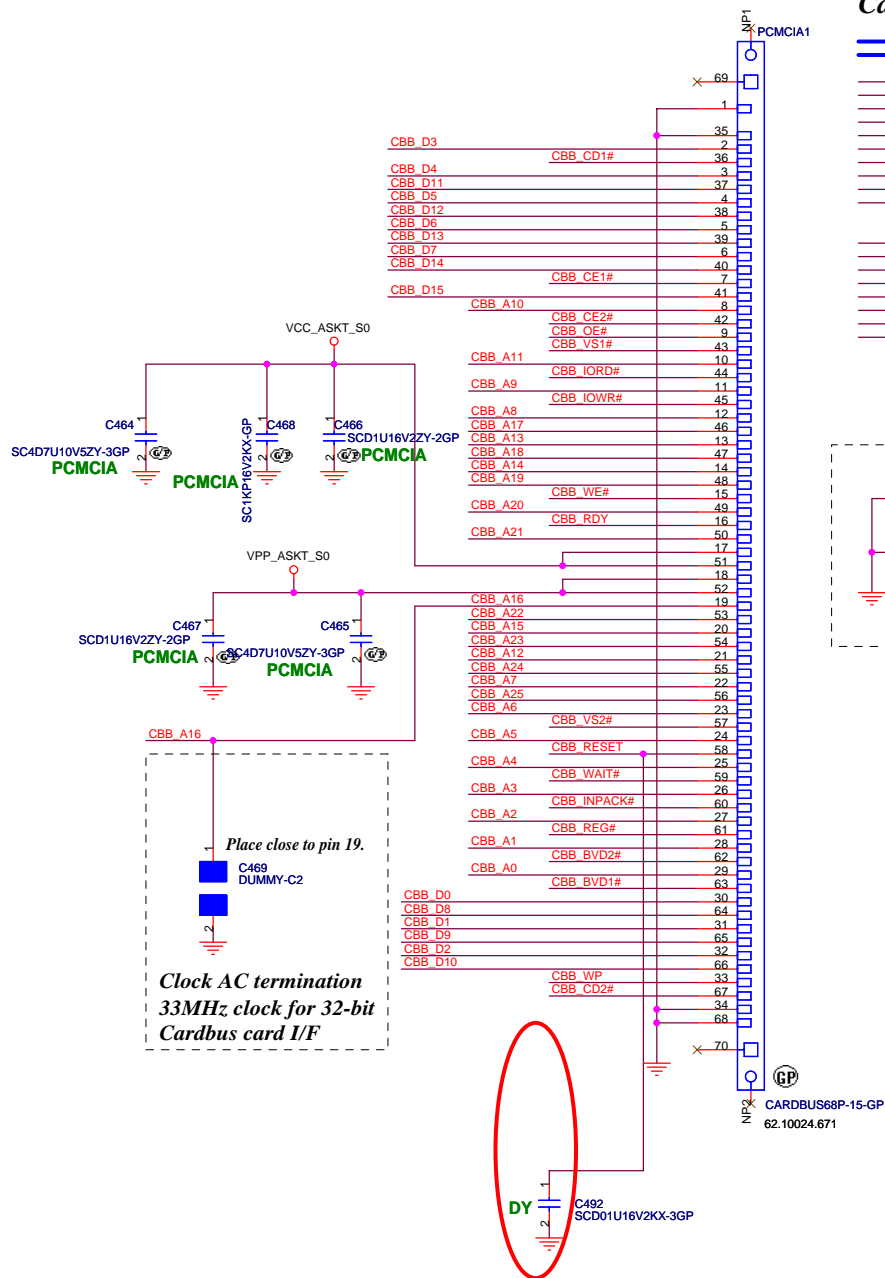
1 36
Reader

Title		MINI CARD / 1394	
Size	Document Number	Rev	
A3	AG1	-1M	
Date: Tuesday, January 10, 2006		Sheet	26 of 53

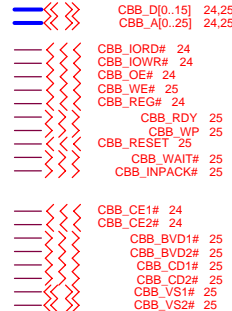
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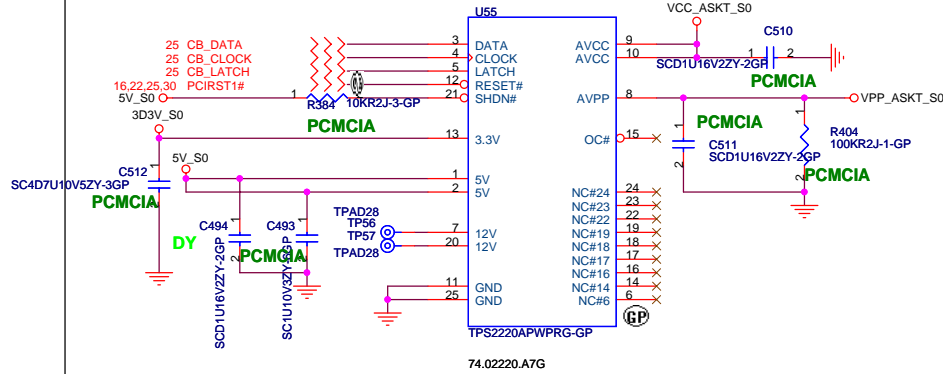
PCMCIA Socket

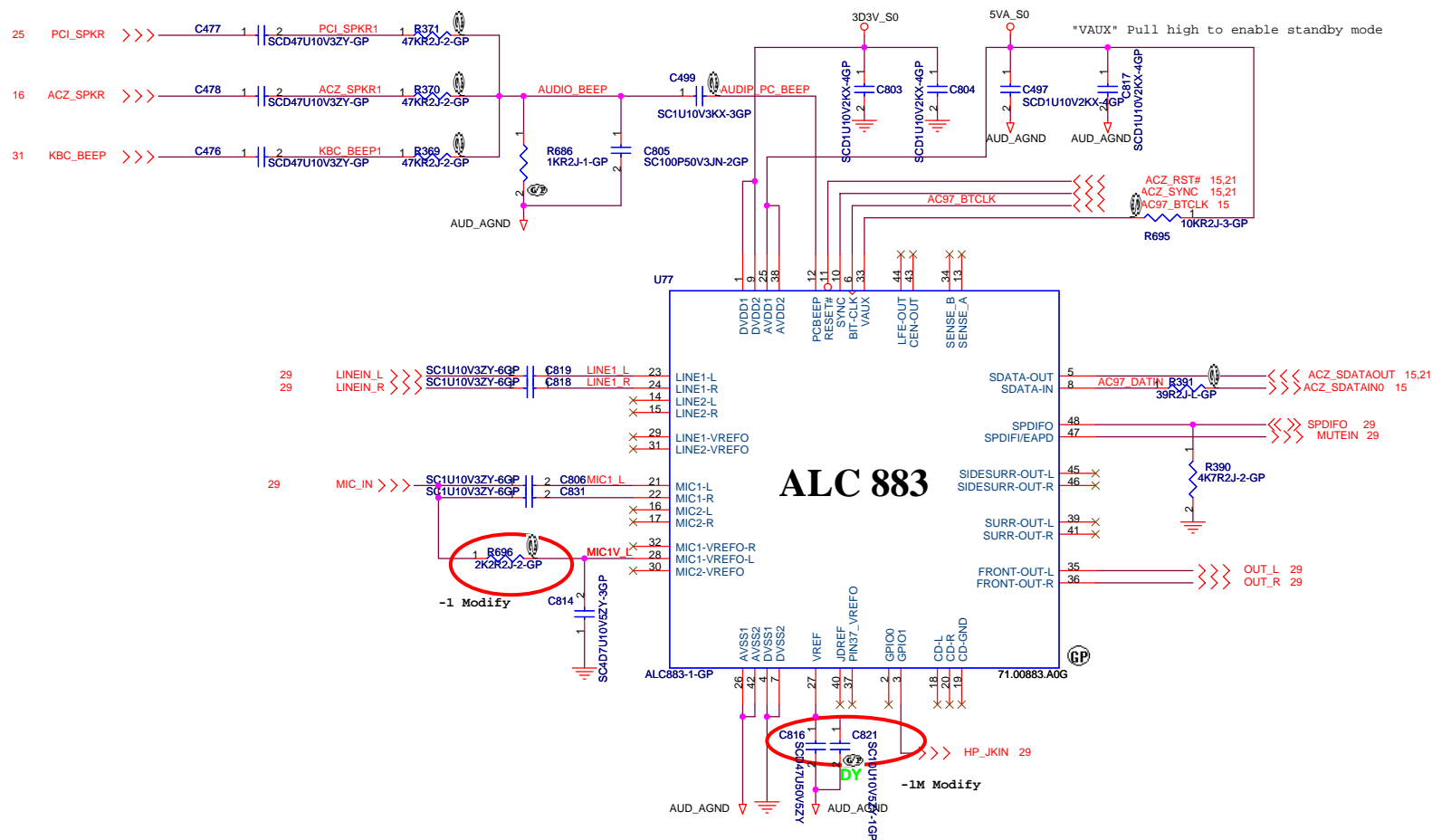


Cardbus I/F



Power switch





- 1) When GPIO0 is asserted, AMP should be muted.
- 2) SPDIFO should be turned off when not used.

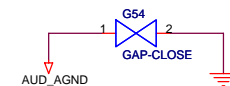
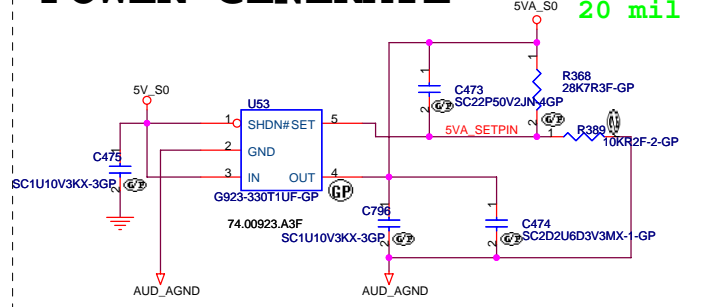
Configuration:

(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP, Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input

POWER GENERATE

Layout
20 mil



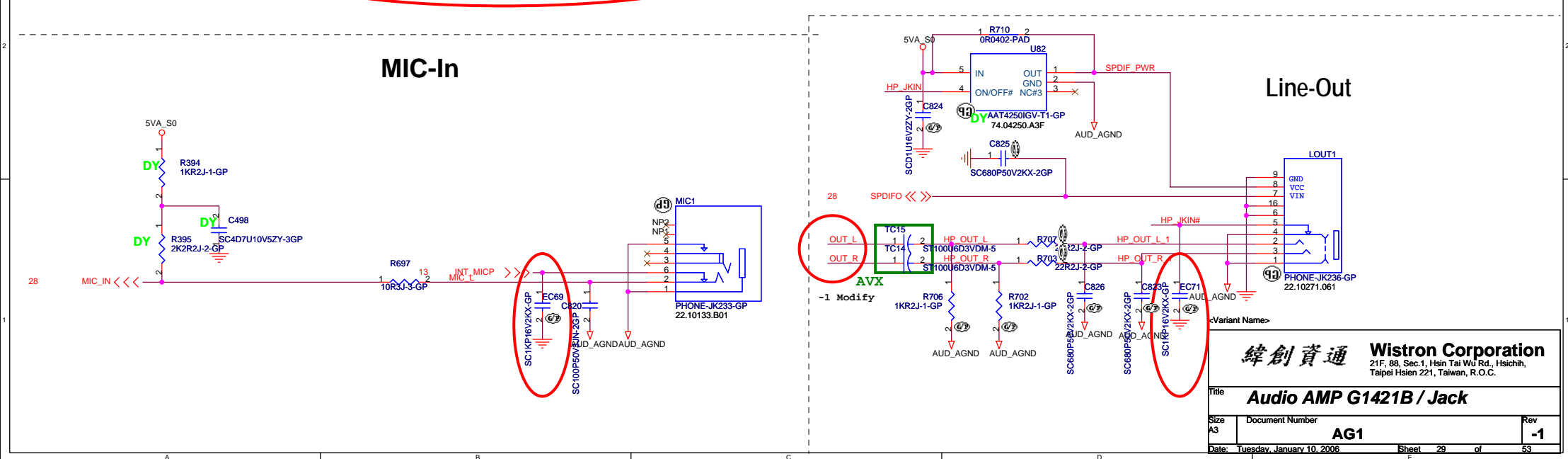
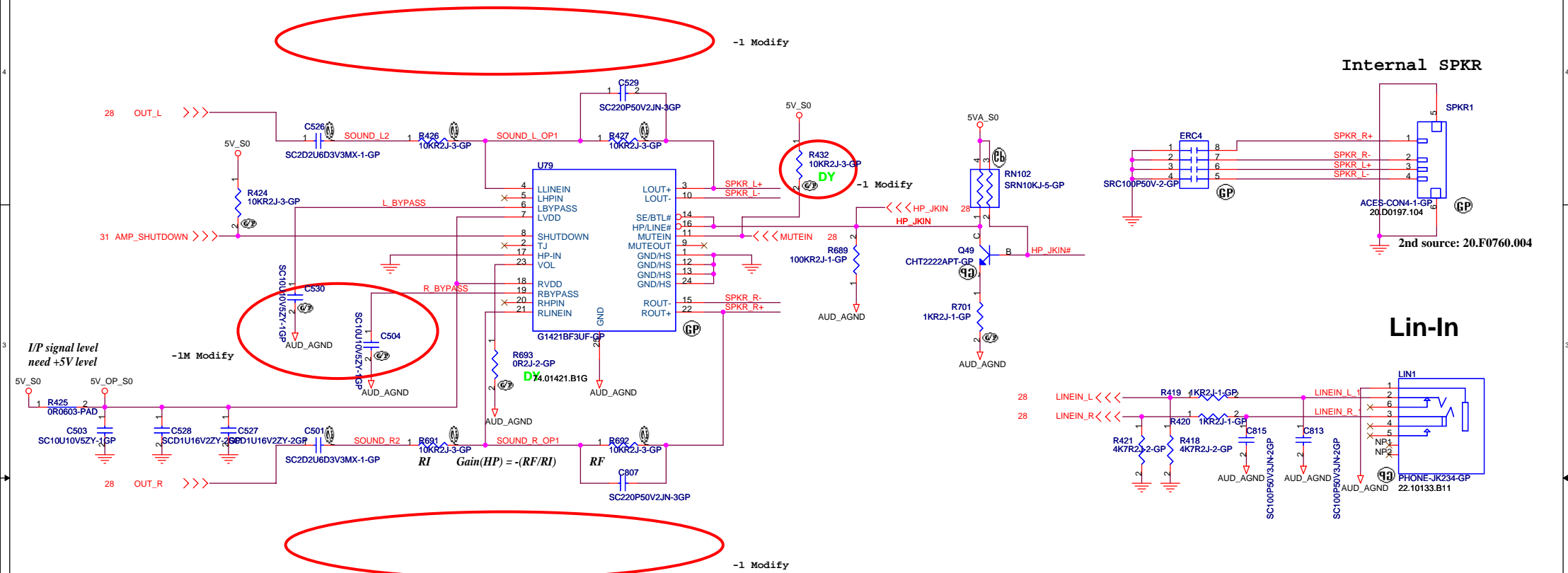
<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

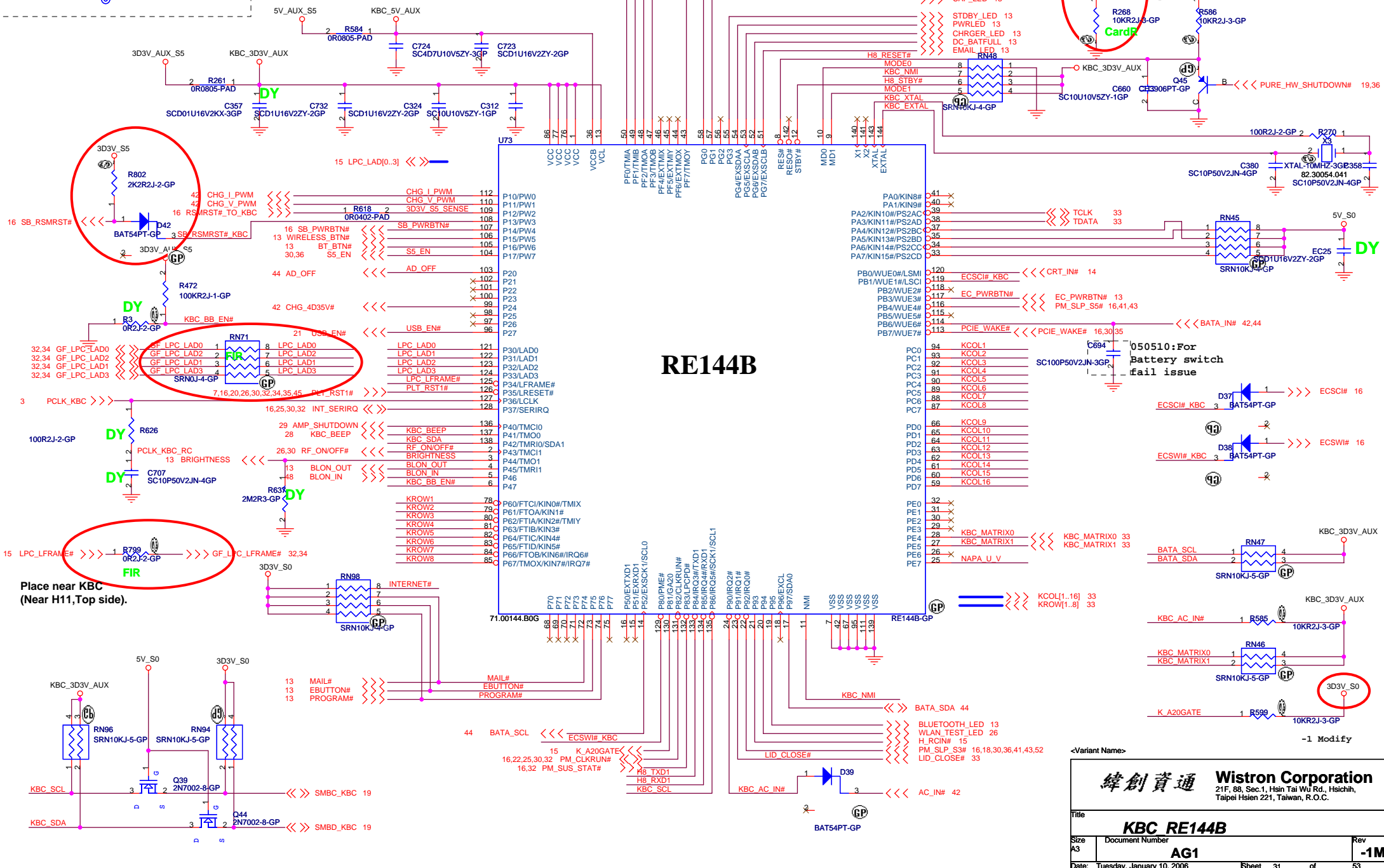
Title **Azalia codec ALC883**

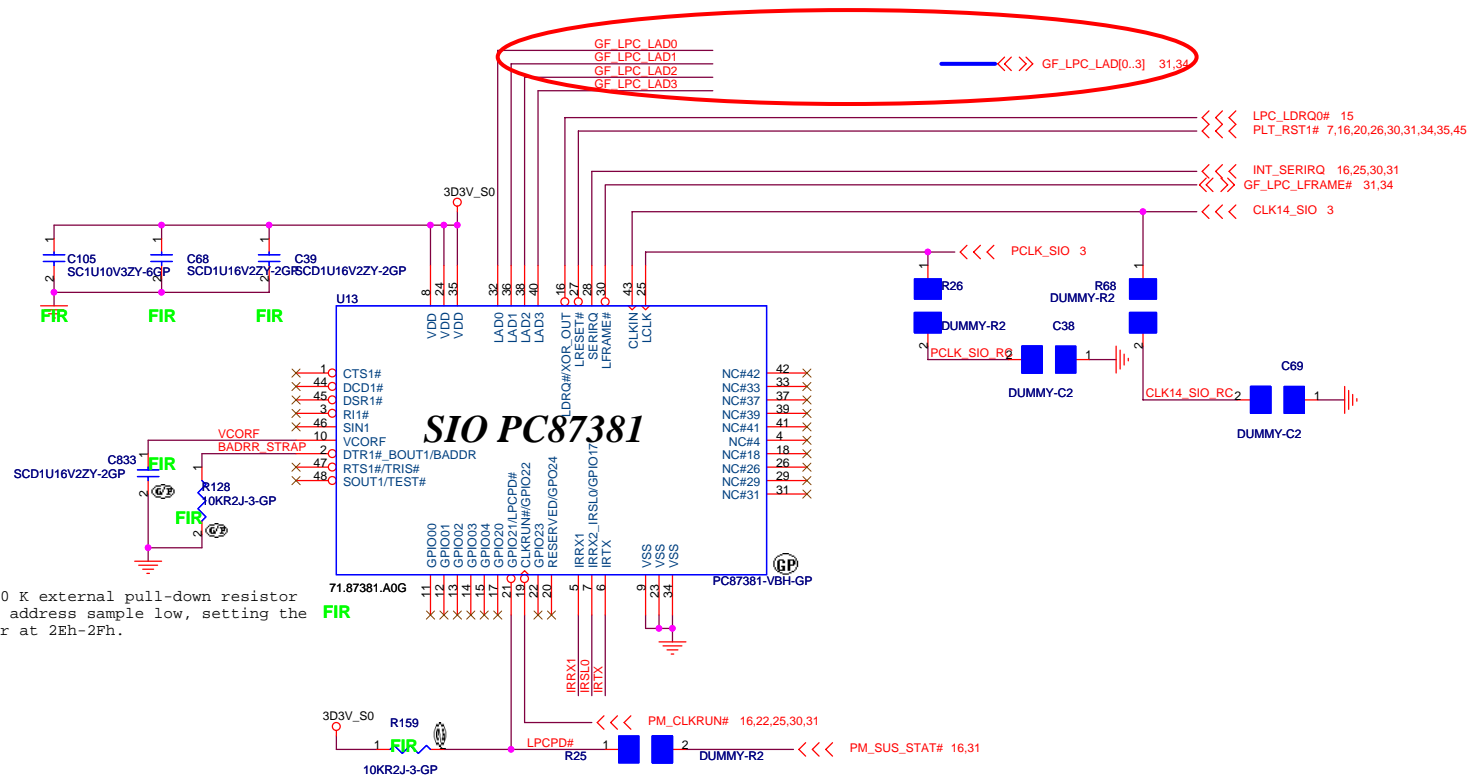
Size A3	Document Number AG1	Rev -1M
Date: Tuesday, January 10, 2006	Sheet 28 of 53	

AUDIO OP AMPLIFIER



Pin No.		Pin No.
1	3D3V_AUX_KBC	2
3	H8_RESET#	4
5	KBC_AC_IN#	6
7	LID_CLOSE#	8
9	PM_SLP_S3#	10

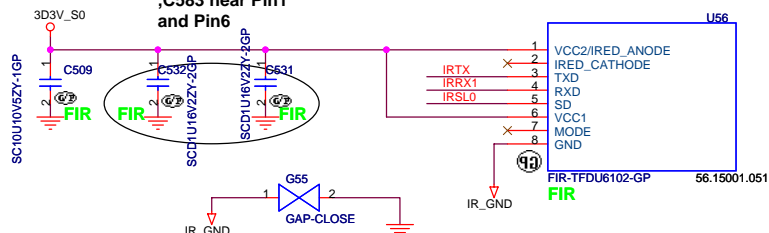




VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32

Place C581
,C583 near Pin1
and Pin6

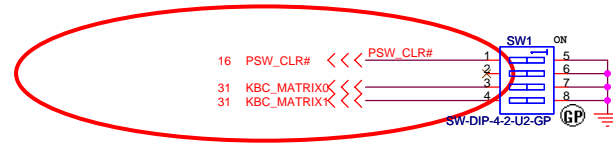


<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
SIO 87381 / FIR		
Size	Document Number	Rev
A3	AG1	-1
Date:	Tuesday, January 10, 2006	Sheet 32 of 53

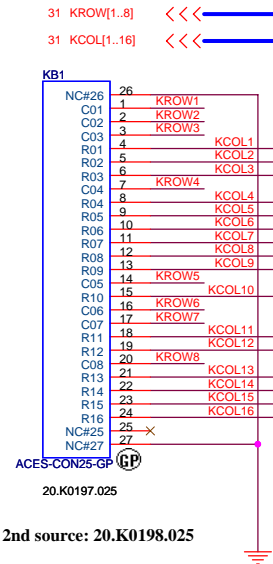
Internal KeyBoard Connector



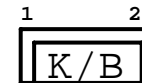
Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

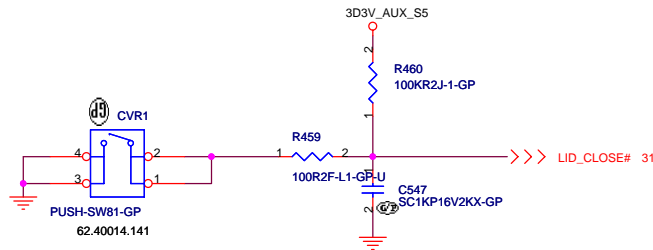
	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON



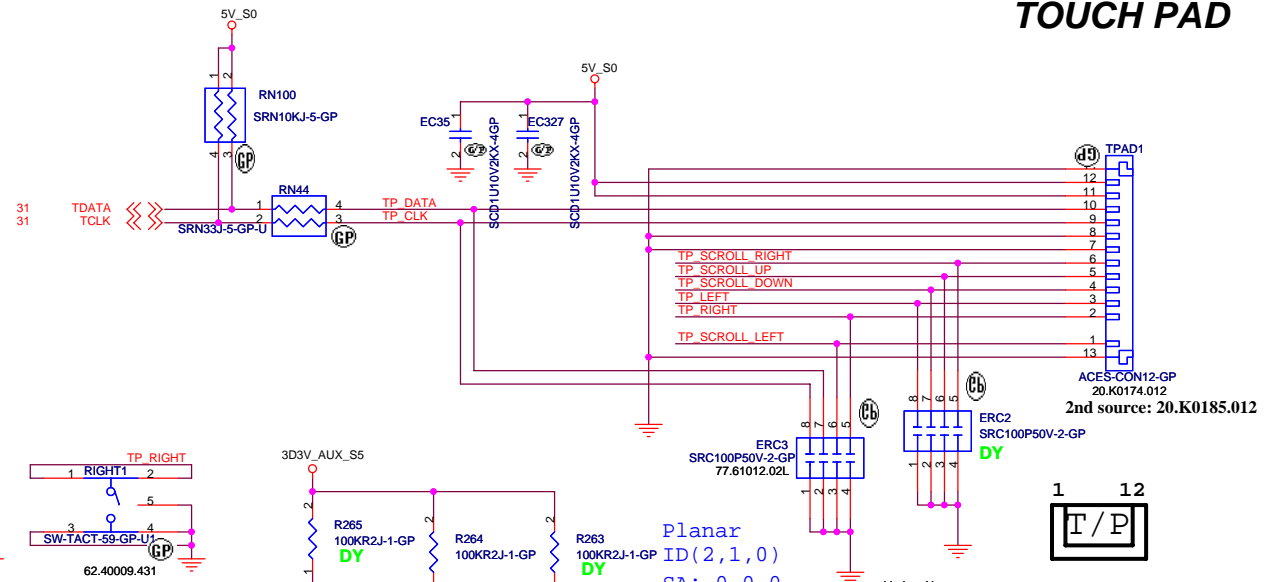
2nd source: 20.K0198.025



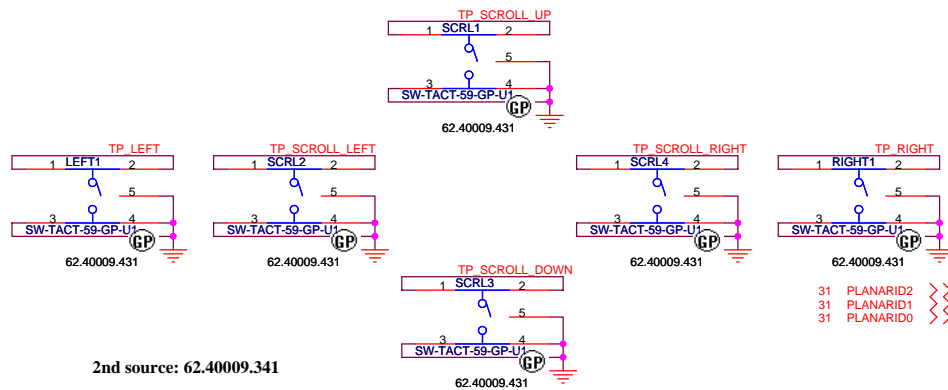
COVER SWITCH



TOUCH PAD



SCROLL KEY



2nd source: 62.40009.431

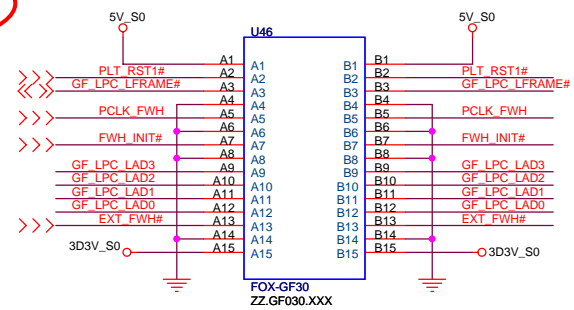
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
-1: 1,0,0

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KEYBOARD/TOUCHPAD	
Title Size A3 Date: Tuesday, January 10, 2006	Document Number AG1 Sheet 33 of 53
Rev SC	

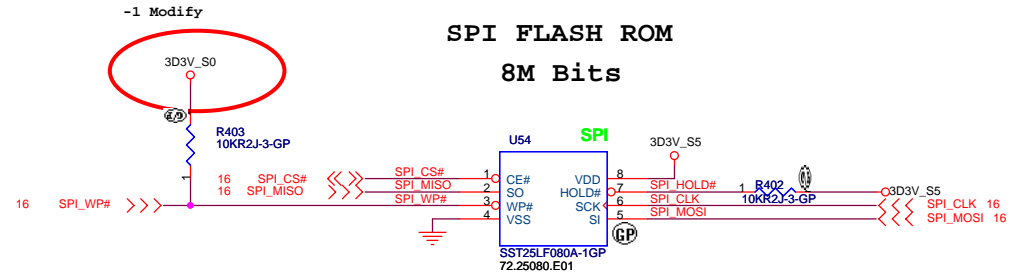
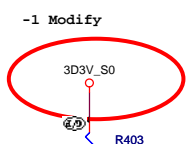


7,16,20,26,30,31,32,35,45 PLT_RST1#
31,32 GF_LPC_LFRAME#
3 PCLK_FWH
15 FWH_INIT#
16 EXT_FWH#

GOLDEN FINGER FOR DEBUG BOARD



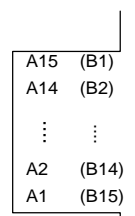
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



SPI FLASH ROM 8M Bits

SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
SST25VF080B : 72.25080.G01
ST M25P80: 72.25P80.001

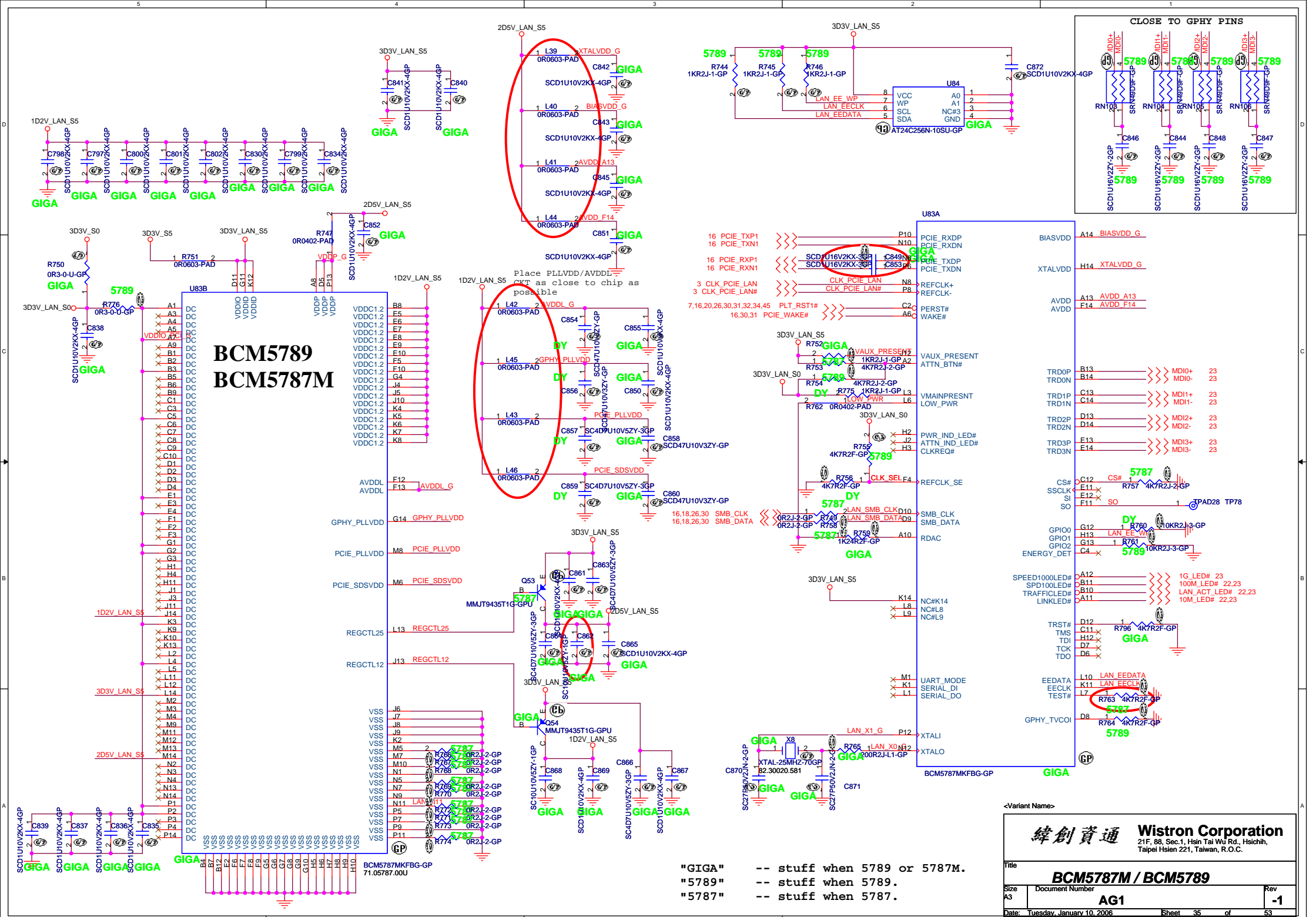
TOP VIEW



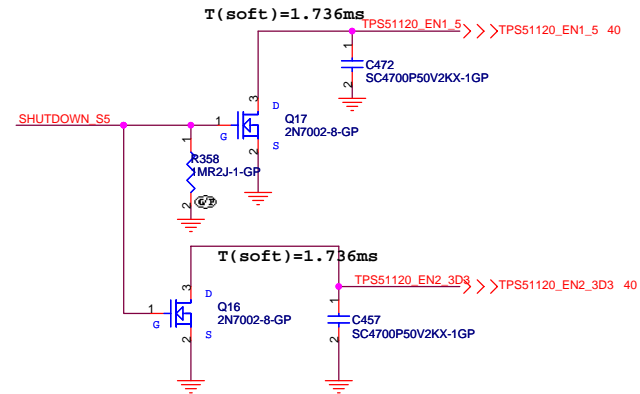
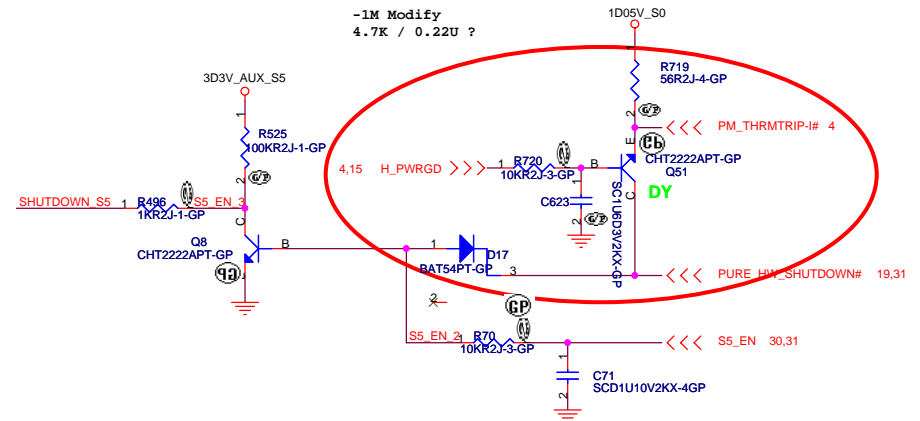
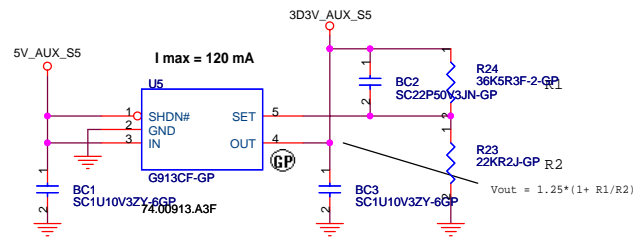
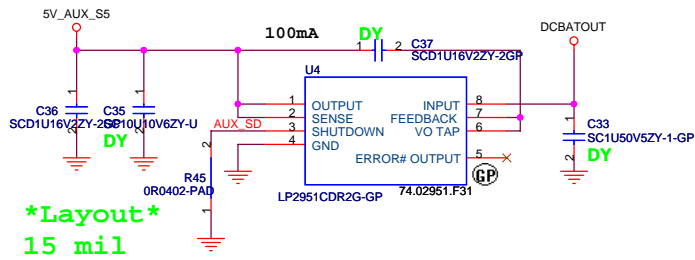
(BOTTOM VIEW)

<Variant Name>

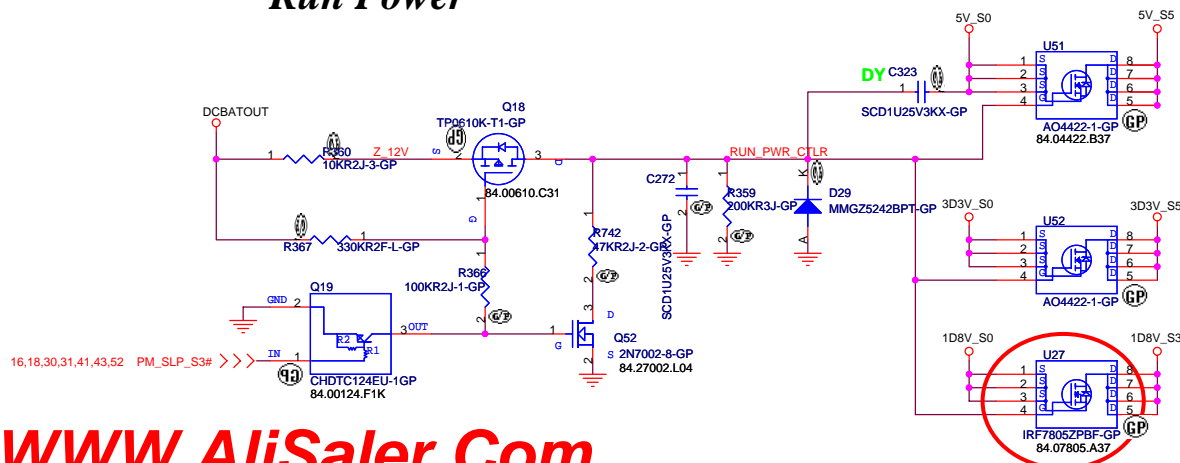
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BIOS : SPI	
Size A3	Document Number AG1
Date: Tuesday, January 10, 2006	Sheet 34 of 53
Rev -1	



Aux Power



Run Power



<Variant Name>

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Title

RUN and AUX POWER

Size
A3

Document Number

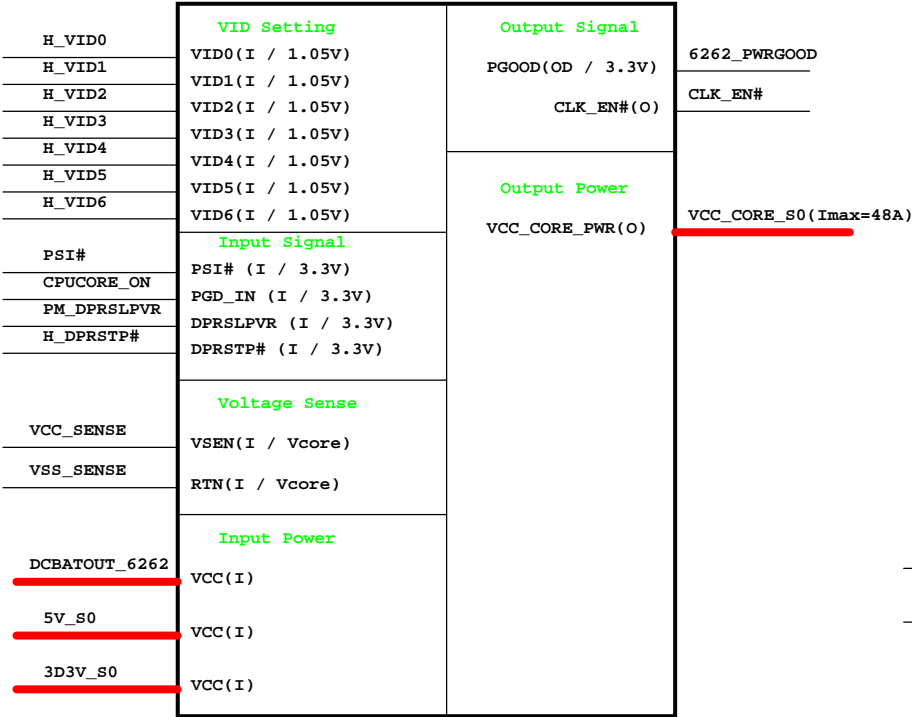
AG1

Rev
-1M

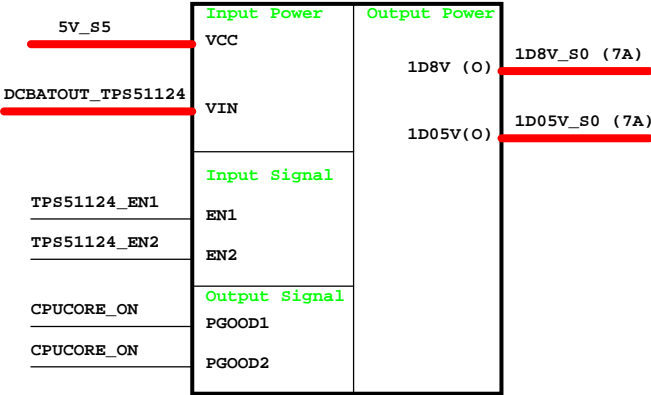
Date: Tuesday, January 10, 2006

Sheet 36 of 53

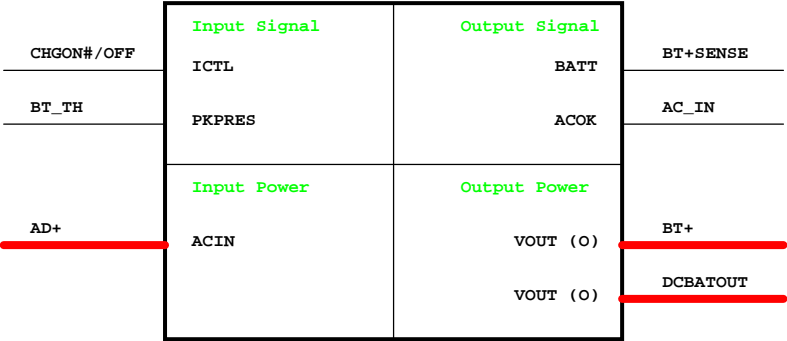
CPU_CORE
Intersil ISL6262



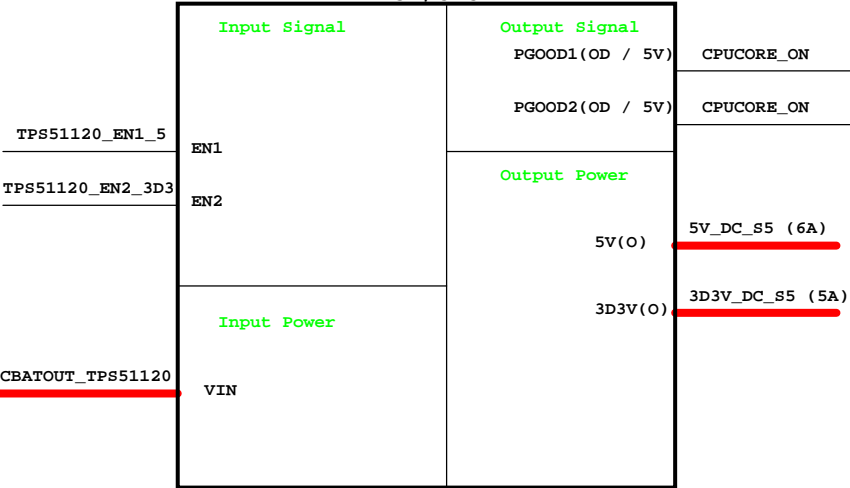
TPS51124
1D8V/1D05V



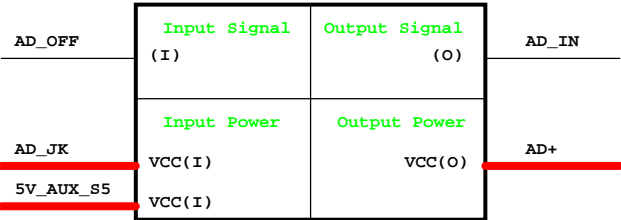
Charger Max8725

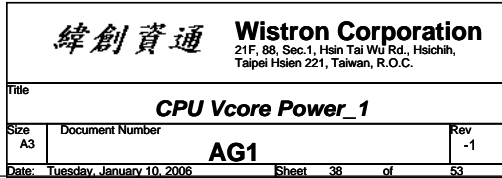


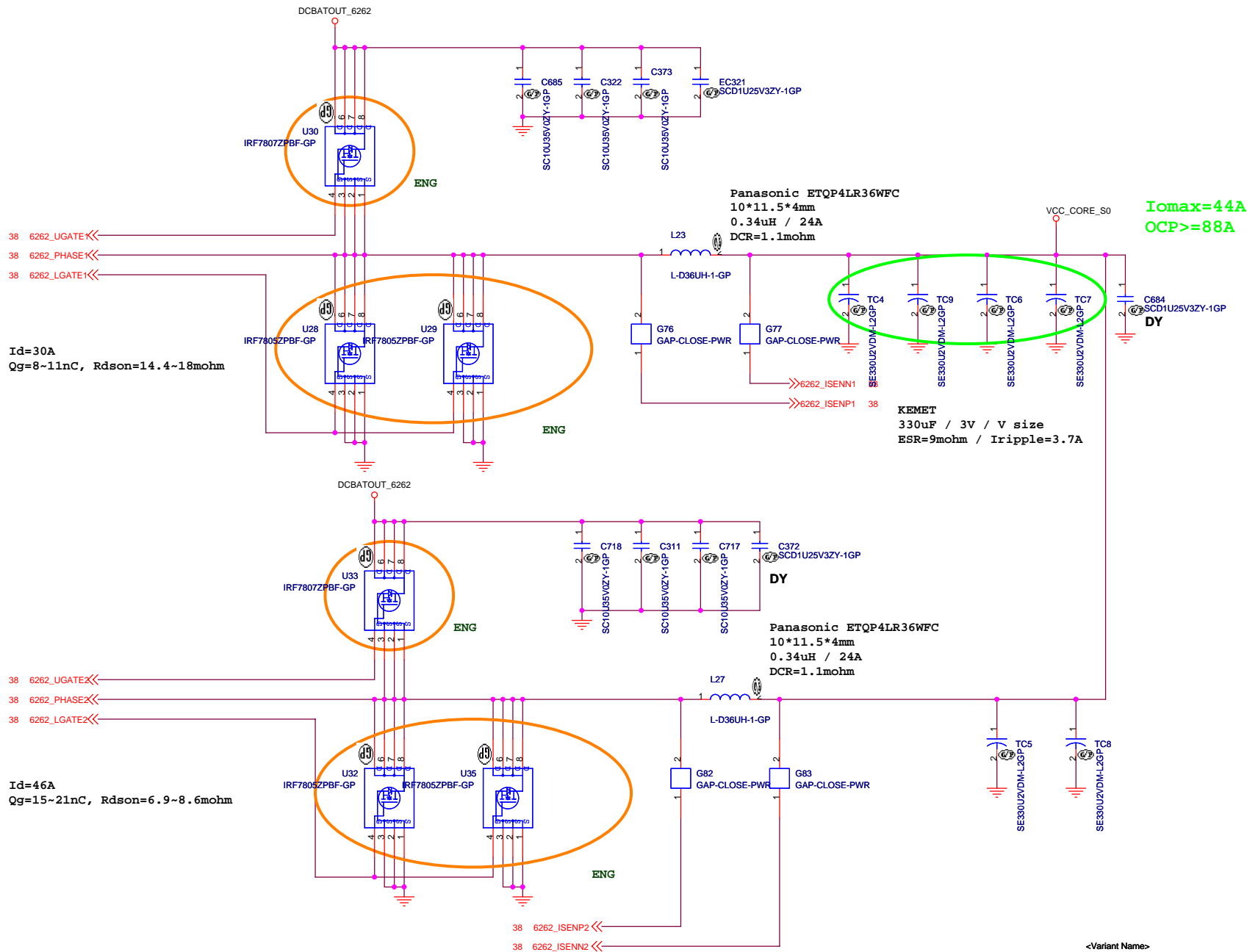
TPS51120
5V/3D3V

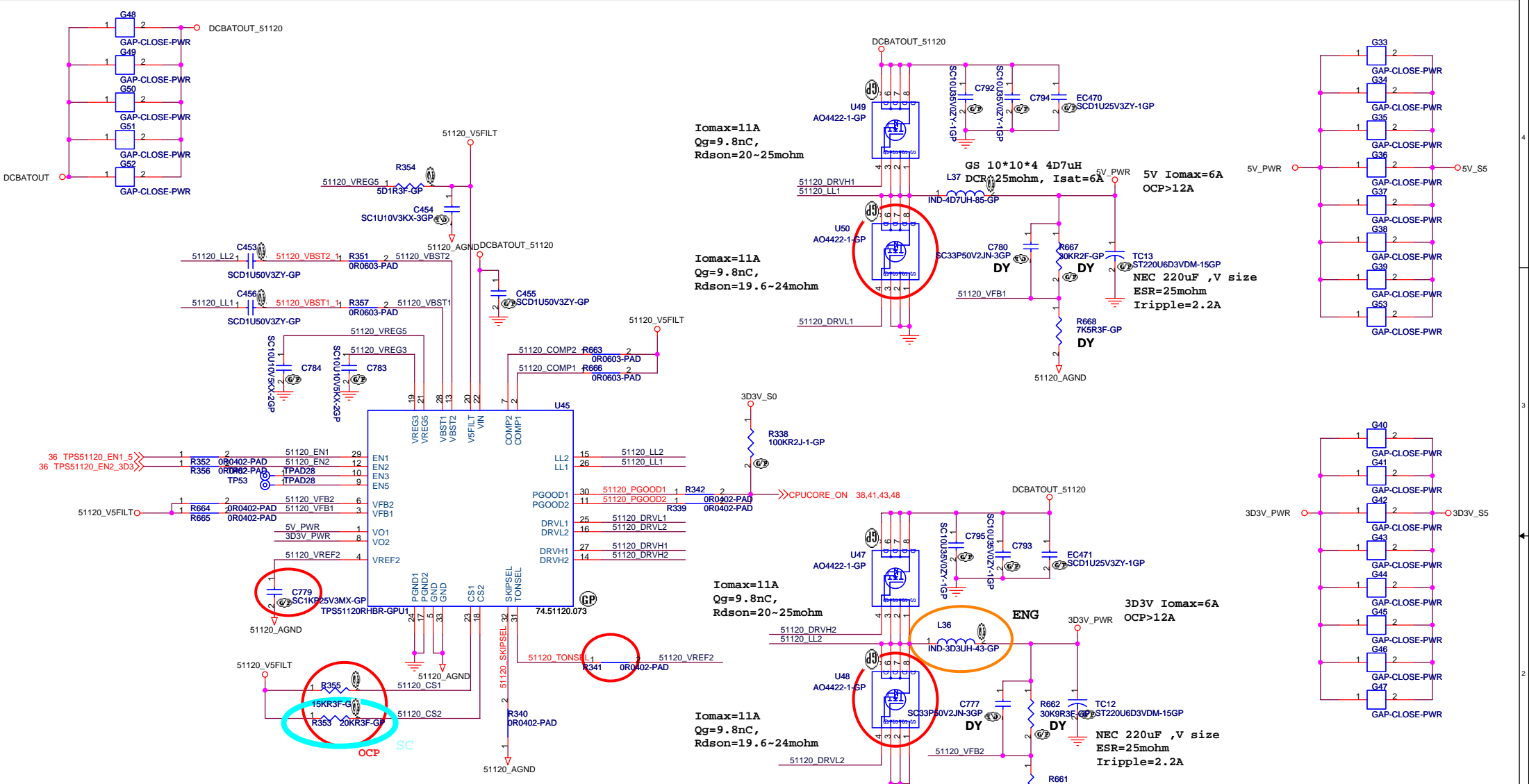


Adapter









	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	not use	not use	DO ON	REG3 on

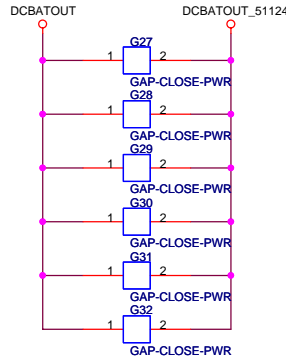
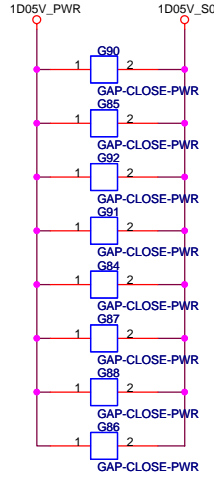
For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

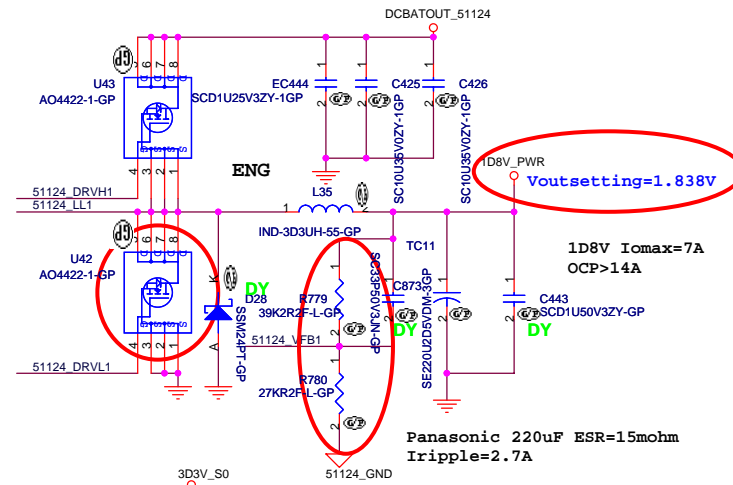
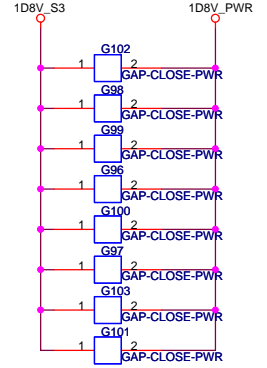
Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

1D05V_S0/7A OCP>=14A



1D8V / 7.0A OCP>=14A



16,31,43 PM_SLP_S5<>>
16,18,30,31,36,43,52 PM_SLP_S3<>>

1D05V Iomax=7A
OCP>14A
Voutsetting=1.051V

$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in}))$

$$V_{out} = 0.75V * (R1 + R2) / R2$$

Panasonic 220uF ESR=15mohm
Irripple=2.7A

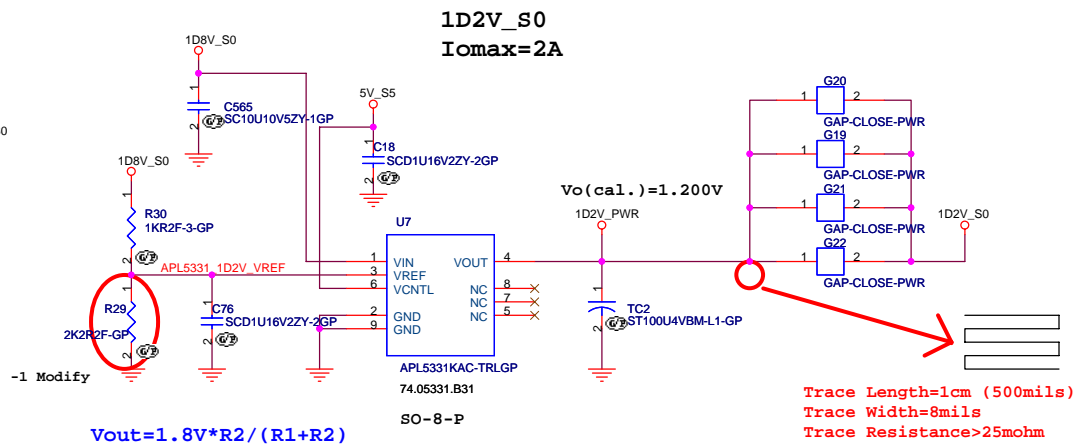
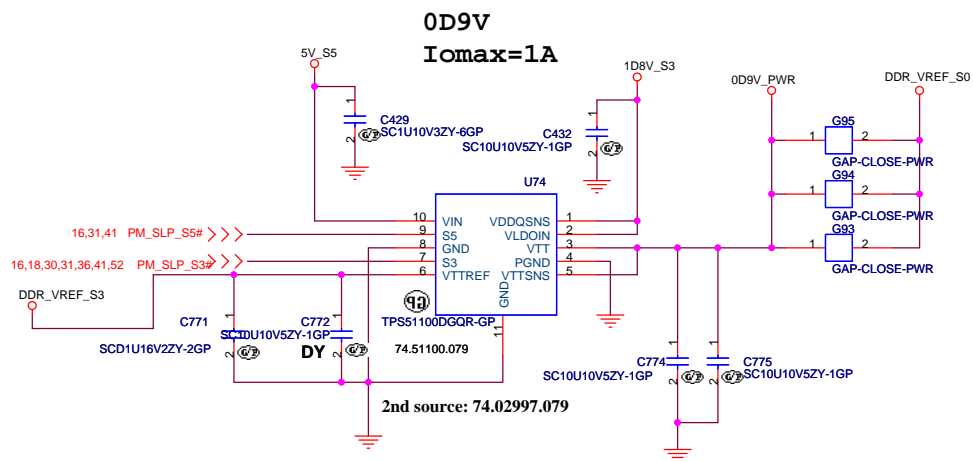
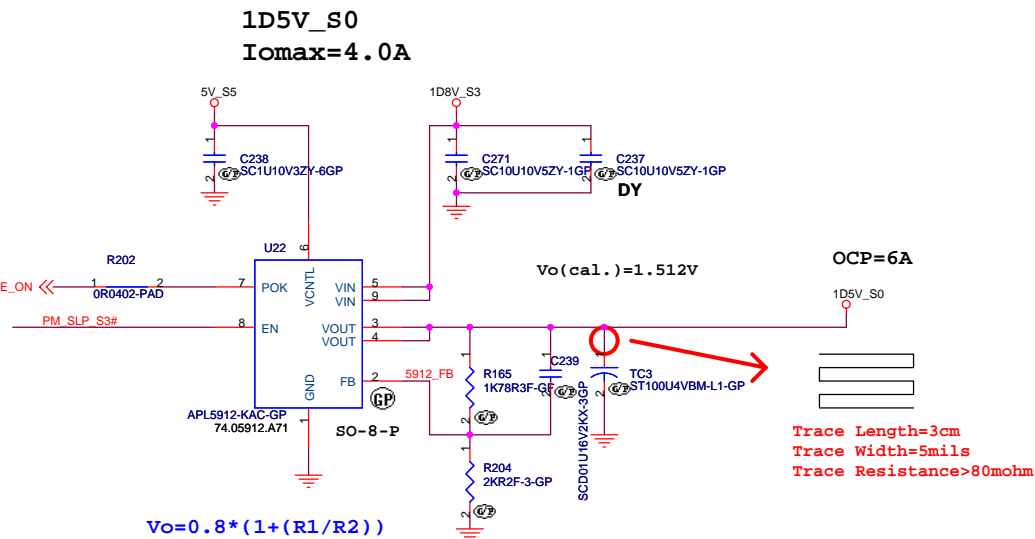
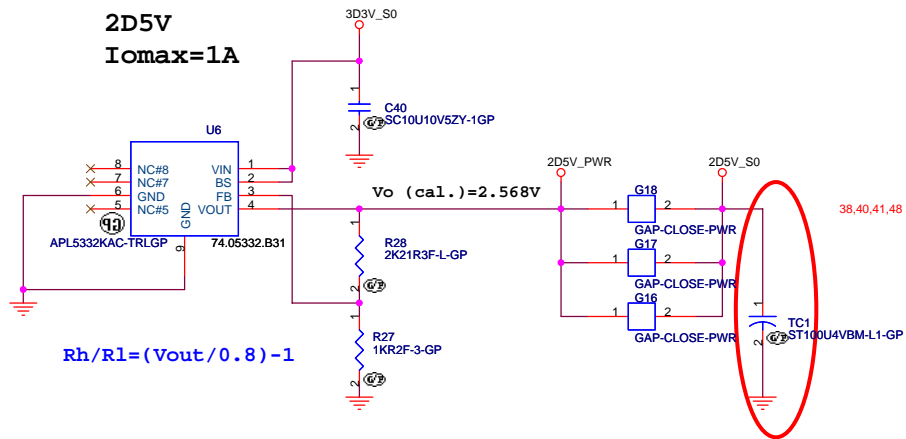
	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

<Variant Name>

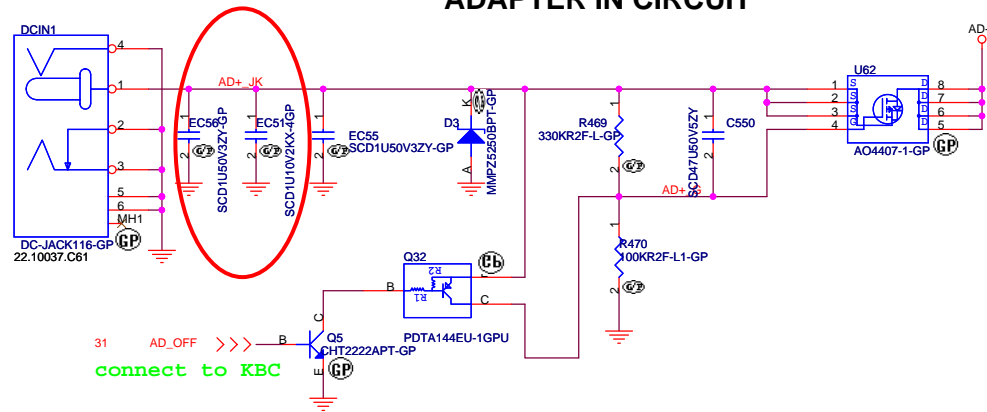
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

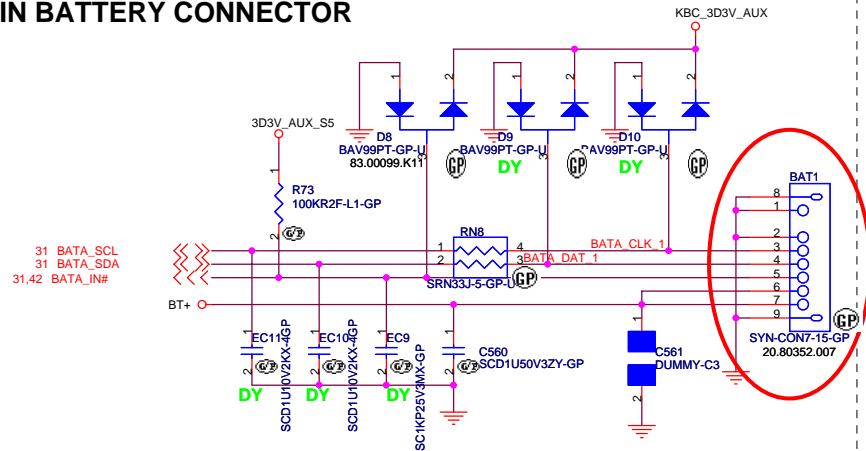
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TPS51124 1D8V_S3/1D05V_S0			
Size	Document Number	Rev	
A3	AG1	-1	
Date:	Tuesday, January 10, 2006	Sheet	41 of 53



ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



<Variant Name>

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Title

AD/BATT CONN

Size
A3

Document Number

AG1

Rev
-1

Date: Tuesday, January 10, 2006

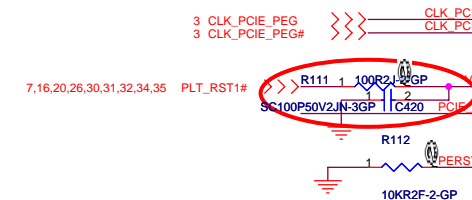
Sheet 44 of 53

PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

7 PEG_RXP[15..0] <<< PEG_RXP[15..0]
7 PEG_RXN[15..0] <<< PEG_RXN[15..0]
7 PEG_TXP[15..0] >>> PEG_TXP[15..0]
7 PEG_TXN[15..0] >>> PEG_TXN[15..0]

PCIE SIGNALS CONNECT TO ROOT COMPLEX

REFER TO PCI EXPRESS DESIGN GUIDE
FOR RECOMMENDED AC COUPLING CAPS
PLACEMENT ALONG THE TX INTERCONNECT



M54P: 71.0M54P.A0U
M56P: 71.0M56P.B0U

VGA THERMAL SENSOR



Place near GPU

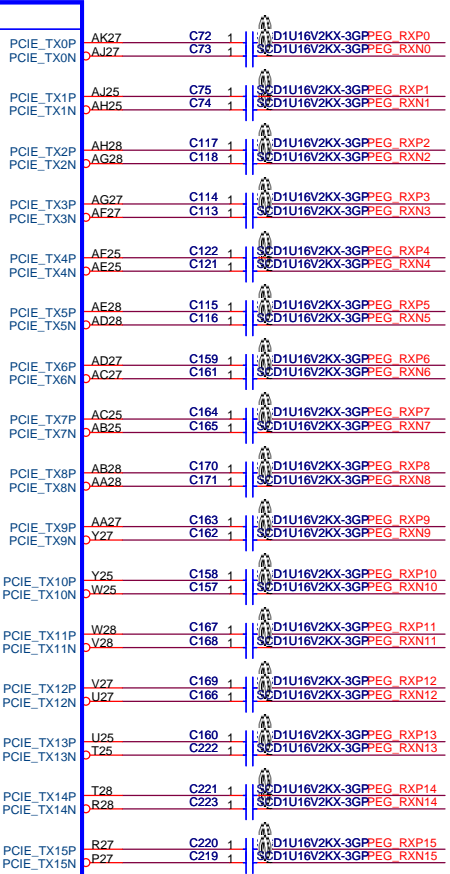
IT IS REQUIRED TO DESIGN IN A THERMAL SENSOR
TO FACILITATE THERMAL EVALUATION AND TO PROTECT THE ASIC

P
C
I
E
-
E
X
P
R
E
S
S

I
N
T
E
R
F
A
C
E

U70A

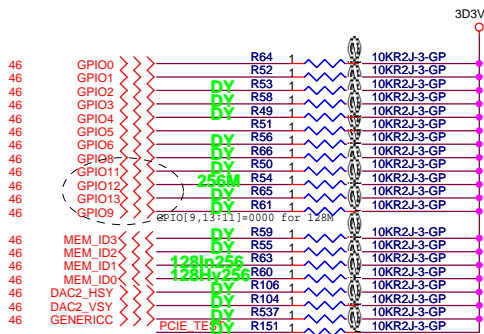
PART 1 OF 7



FOR M26X
PCIE_CALRN = 100R
PCIE_CALRP = 150R
PCIE_CALI = 10K
FOR M52P,M54P,M56P
PCIE_CALRN = 2K
PCIE_CALRP = 562R
PCIE_CALI = 1.47K

MEM_ID0	MEM_ID2	MEM_ID1	MEM_ID3	MEM	SIZE	VENDOR	CHIPS
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Infineon	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	128M	16M*16	Hynix	x4
1	0	0	0	256M	32M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3,2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0)	GPIO[9,13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM	1011
MEMORY APERTURE SIZE	GPIO[13:11]	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERTURE SETTINGS	TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	



When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

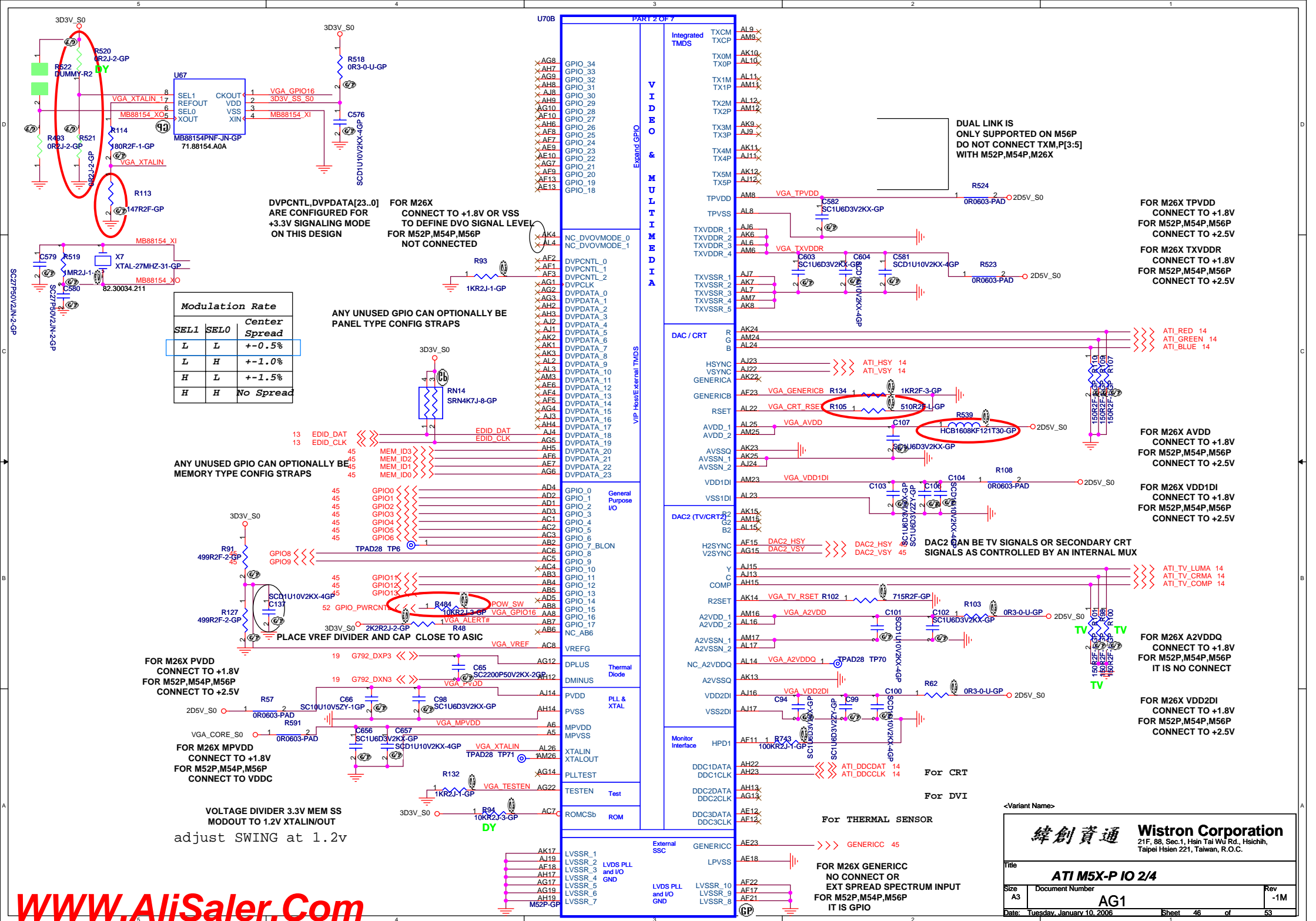
<Variant Name>

緯創資通

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Title		
ATI M5X-P PCIE 1/4		
Size	Document Number	Rev
A3	AG1	SD
Date: Tuesday, January 10, 2006	Sheet 45 of 53	



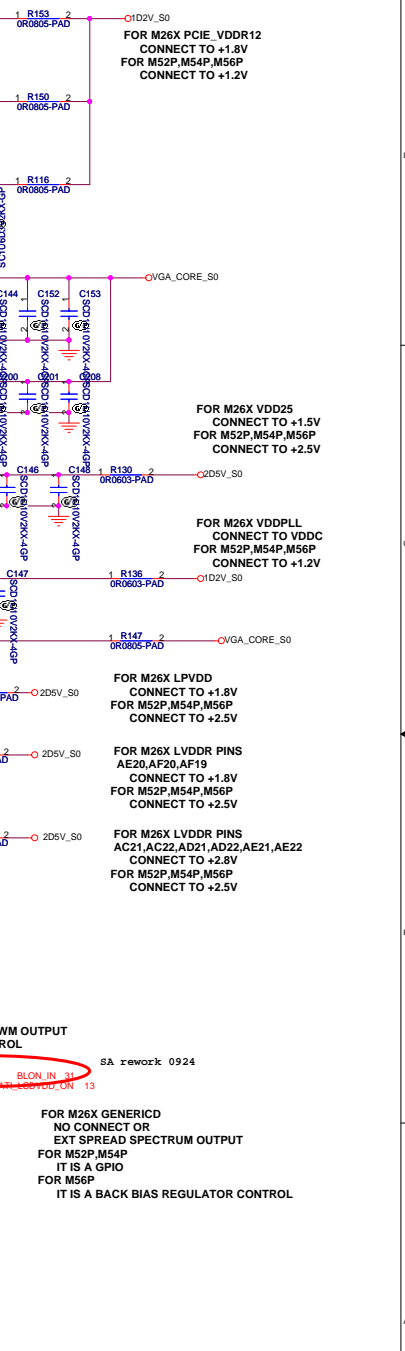
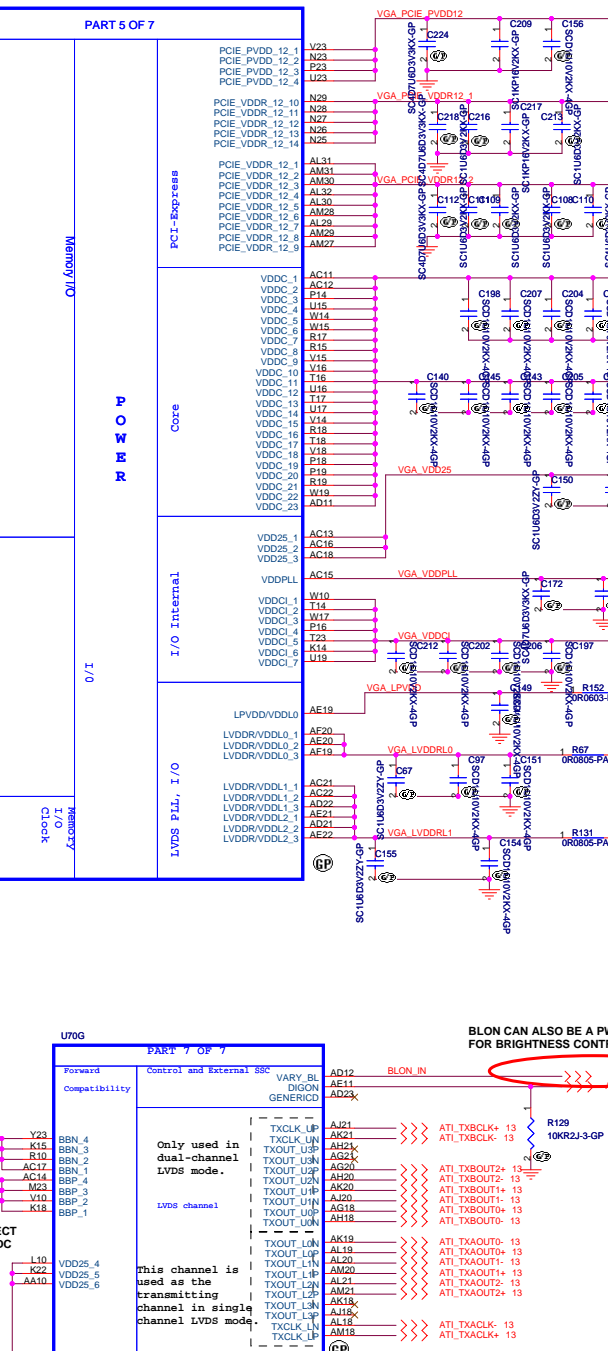
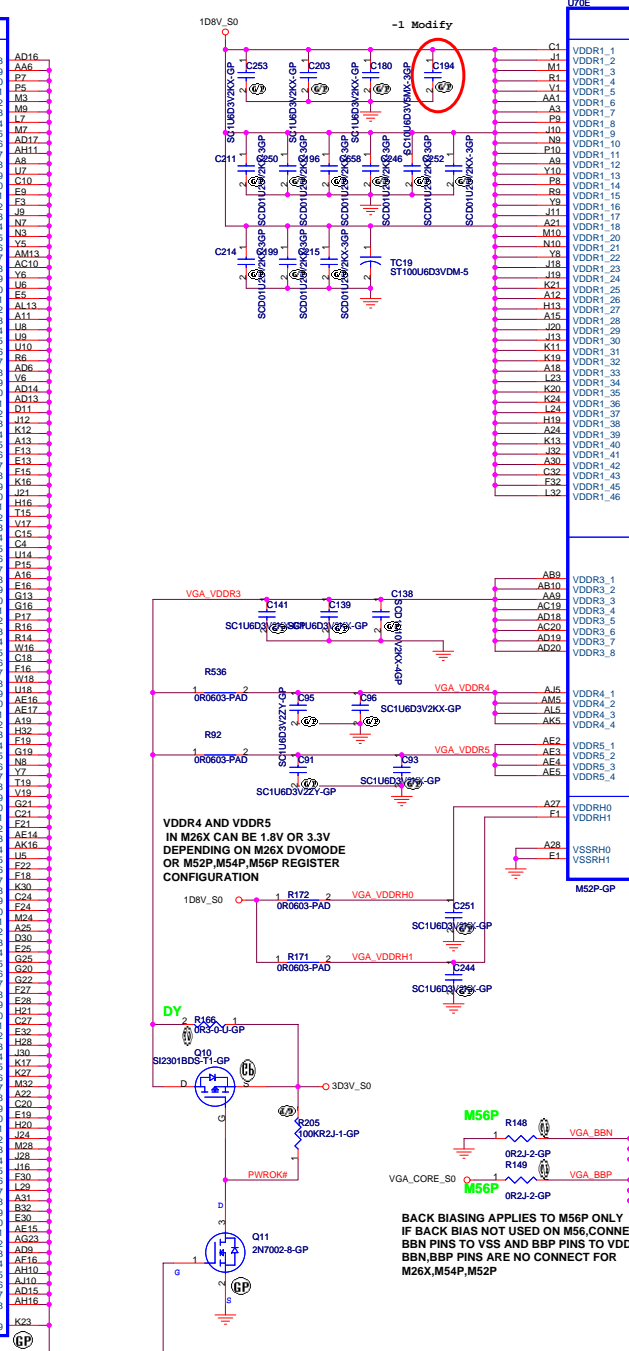
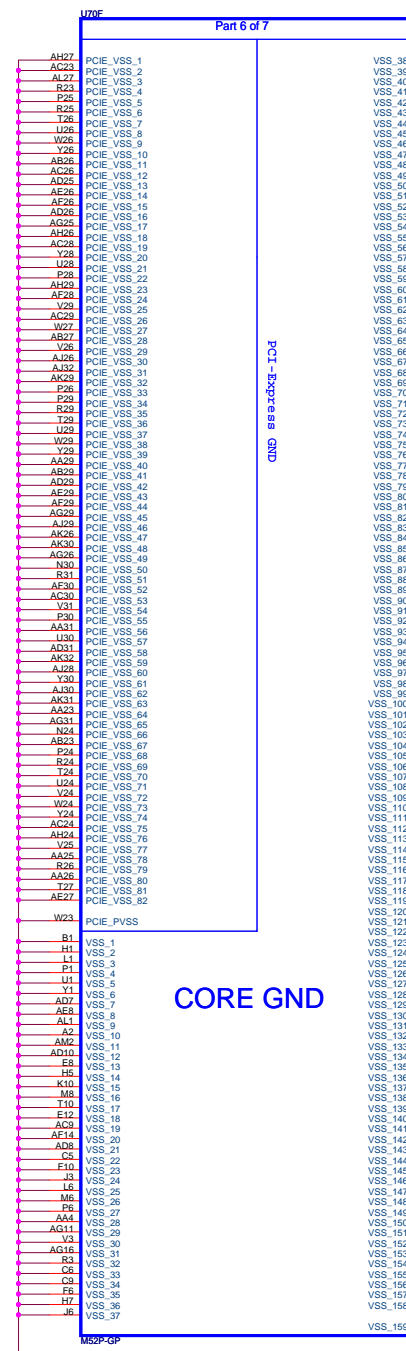


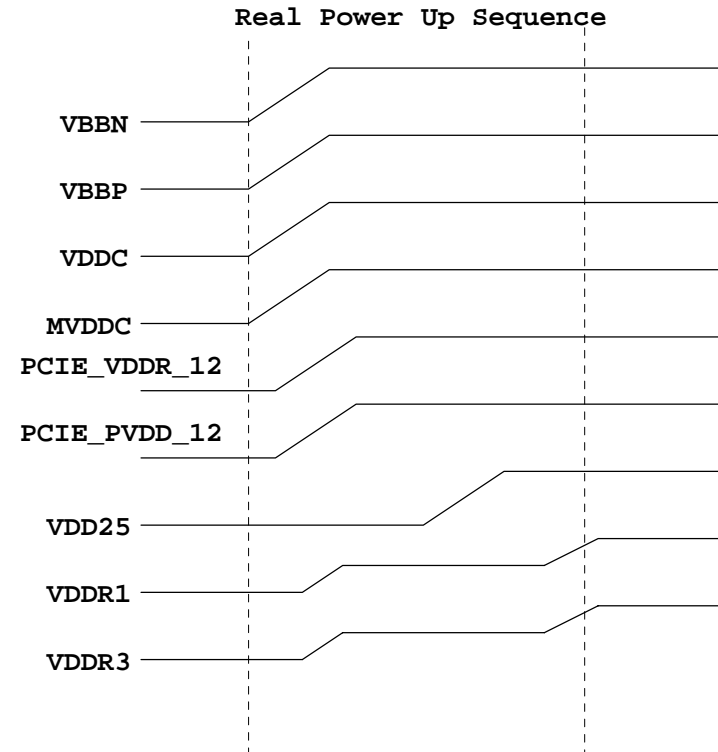
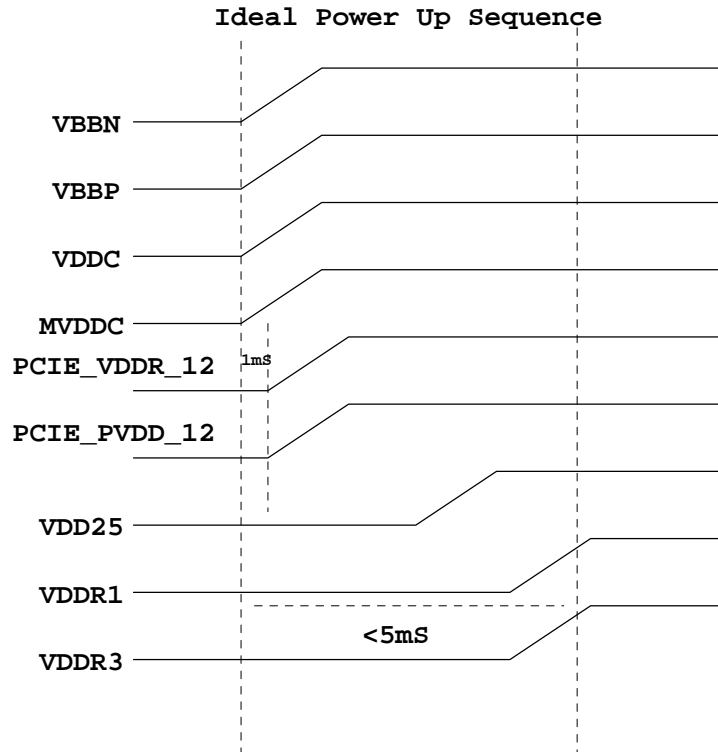
PLACE MVREF DIVIDER AND CAPS CLOSE TO A



<Variant Name>

Title			
ATI M5X-P MEM 3/4			
Size A3	Document Number		Rev
	AG1		SC
Date:	Tuesday, January 10, 2006	Sheet 47 of	53





RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,.....

General Guidelines:

- BBN and BBP must ramp up before or at the same time as VDDC but not after.
- VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_FVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).
- All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).
- VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.
- The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory I/Os) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

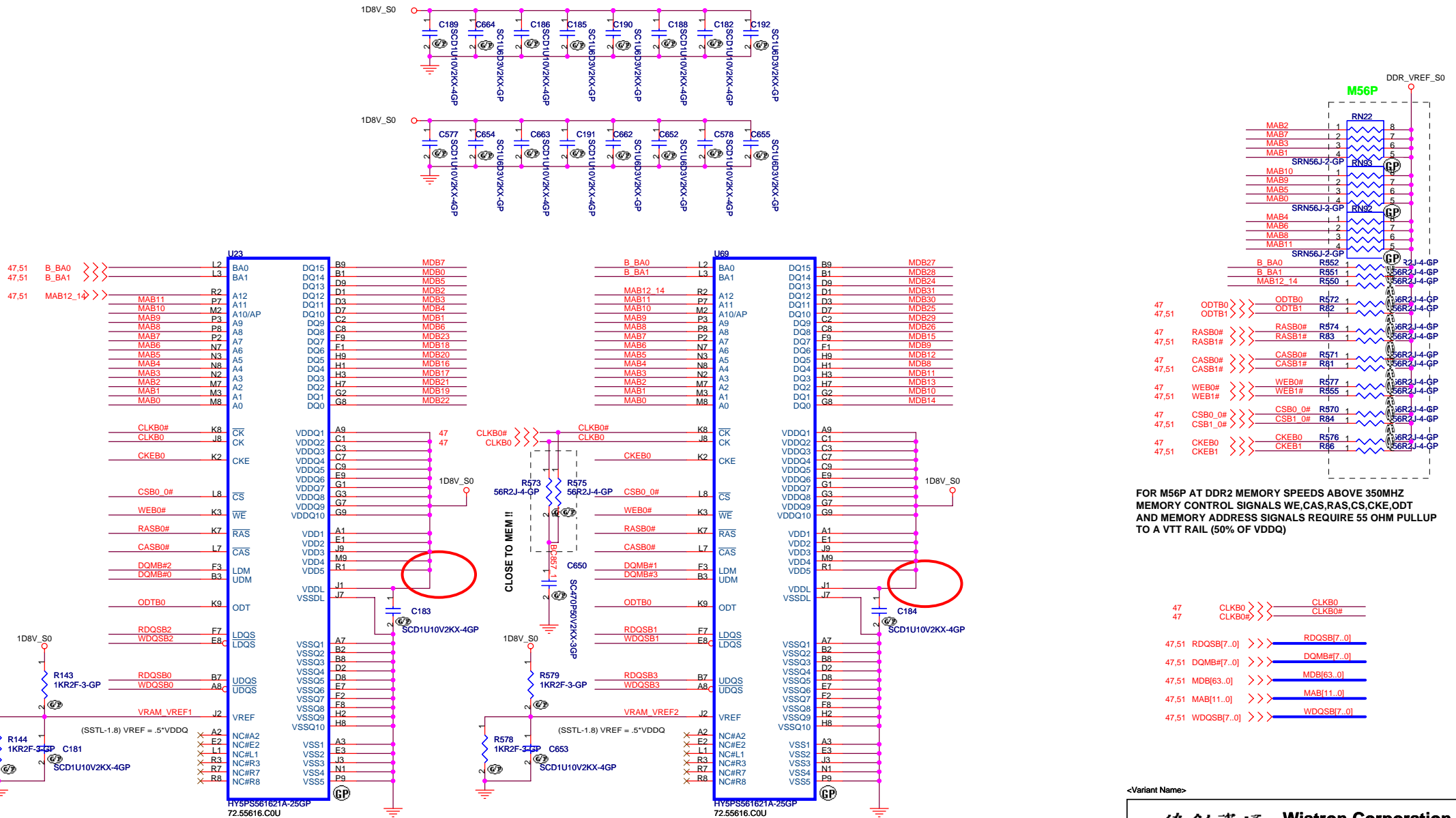
Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

<Variant Name>

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Title			
ATI M5X-P POWER SEQUENCE			
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CHAN B DDR2 84BGA 32MX16 MEMORY



FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ
MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT
AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP
TO A VTT RAIL (50% OF VDDQ)

47 CLKB0# >>> CLKB0#
47 CLKB0# >>> CLKB0#
47,51 RDQSB[7..0] >>> RDQSB[7..0]
47,51 DQMB[7..0] >>> DQMB[7..0]
47,51 MDB[63..0] >>> MDB[63..0]
47,51 MAB[11..0] >>> MAB[11..0]
47,51 WDQSB[7..0] >>> WDQSB[7..0]

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM 1/2**

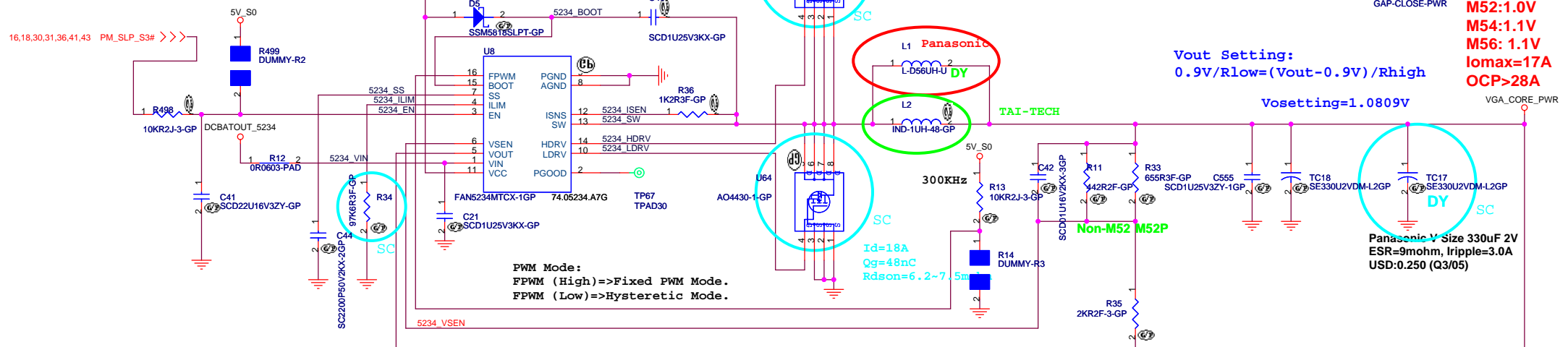
Size: A3 Document Number: **AG1** Rev: SC

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72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 350MHz) Hynix-128M
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA (16M*16, 350MHz) Infineon-128M
72.18512.A0U IC VRAM HYB18T512161BF-25 BGA (32M*16, 400MHz) Infineon-256M

FAN5234 FOR VGA_Core

16,18,30,31,36,41,43 PM_SLP_S3# >>>



PWM Mode:
FPWM (High)=>Fixed PWM Mode.
FPWM (Low)=>Hysteretic Mode.

$$R_{ilim} = (11.2 / I_{lim}) * ((100 + R_{sense}) / R_{dson})$$

POWERPLAY:

: 1.0V
high (3.3V) = set lower core voltage (e.g. VDDC = 1.0V)
low (0V) = set higher core voltage (e.g. VDDC = 1.2V)
High : R35 + R31 set Vout to 0.9994V.
Low : R35 set Vout to 1.19925V.

M54/M56 : 0.95V

High : R35 + R31 set Vout to 1.0989V.
Low : R35 set Vout to 0.9503V.

M52 : 0.95V, but don't card it.(1.0V)
don't mount Q9
R35 + R31 set Vout to 0.9994V.

ATI M5x VGA Core				
VGA	Ver.	Normal	PowerPlay	
M52	A12	1.0	0.95/1.0	
M54	A12	1.1	0.95/0.95	
		1.2	0.95	
M56	B24	1.1	0.95/0.95	

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
VGA CORE 1D1V	
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